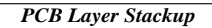


Ver. -1



L1: Signal 1
L2: VCC
L3: Inner Signal 2
L4: Inner Signal 3
L5: GND
L6: Signal 4

CPU V_CORE

ISL6264 38/39

INPUT	OUTPUT
<i>DCBATOUT</i>	<i>VCC_CORE_S0</i>

SYSTEM DC/DC
TPS51124 4

INPUT	OUTPUT
<i>DCBATOUT</i>	<i>1D2V_S0</i> <i>1D8V_S3</i>

SYSTEM DC/DC
ISL6236 4

INPUT	OUTPUT
<i>DCBATOUT</i>	<i>5V_S5</i> <i>3D3V_S5</i>

SYSTEM LDO
TPS51100

INPUT	OUTPUT
1D8V_S3	0D9V_S3

SYSTEM LDO
APL5915

INPUT	OUTPUT
3D3V_S5	1D2V_S5
3D3V_S0	2D5V_S0
3D3V_S0	1D5V_S0

SYSTEM LDO
ISL6236

INPUT	OUTPUT
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5

Battery Charger

ISL6255 42

INPUTS	OUTPUTS
$AD+$ $BAT+$	$DCBATOUT$

UMA



Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title	BLOCK DIAGRAM
-------	---------------

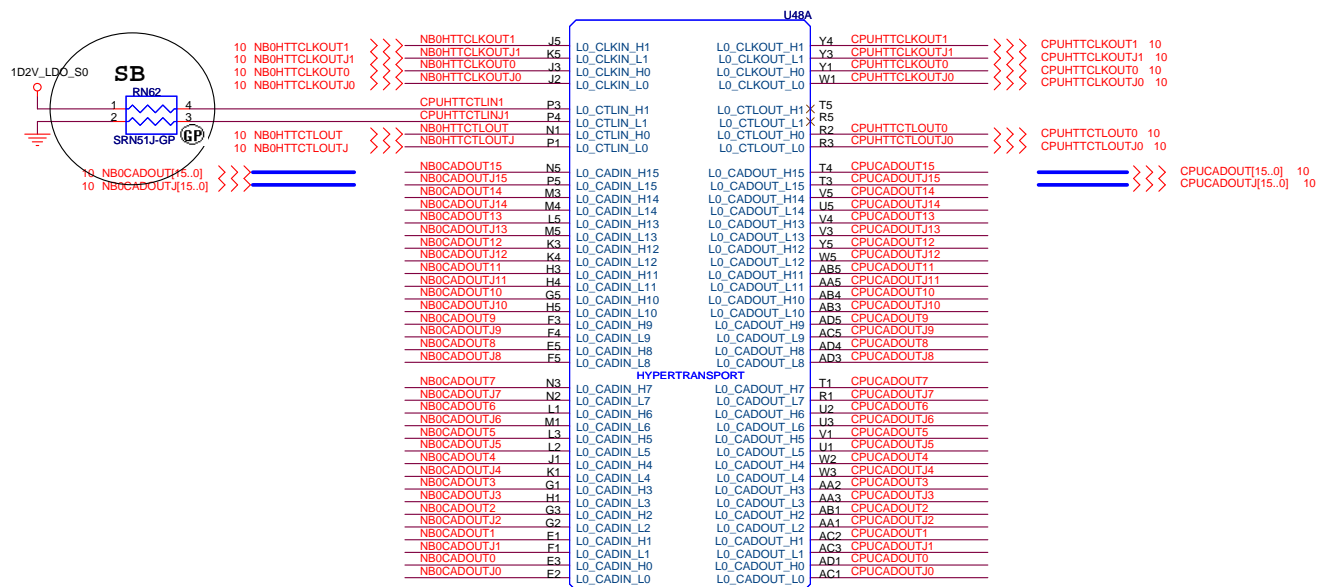
Size A3	Document Number POMONA/TEXCOCO
------------	--

Date: Thursday, March 29, 2007 Sheet 1 of 49

SA: 07/31/06 Start

UMA

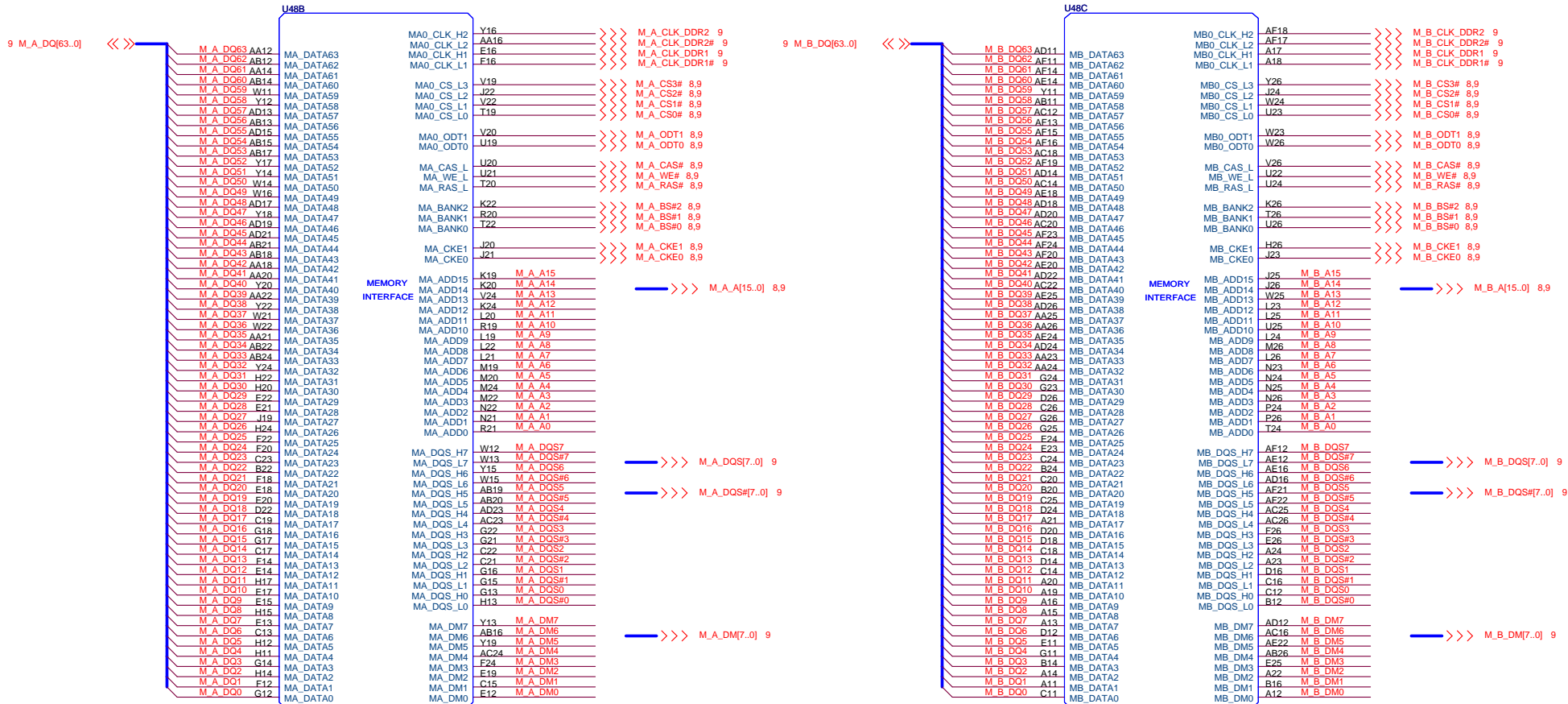
<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
CHANGE HISTORY		
Size	Document Number	Rev
A3	Pomona/Texcoco	1
Date: Thursday, March 29, 2007		Sheet 2 of 49

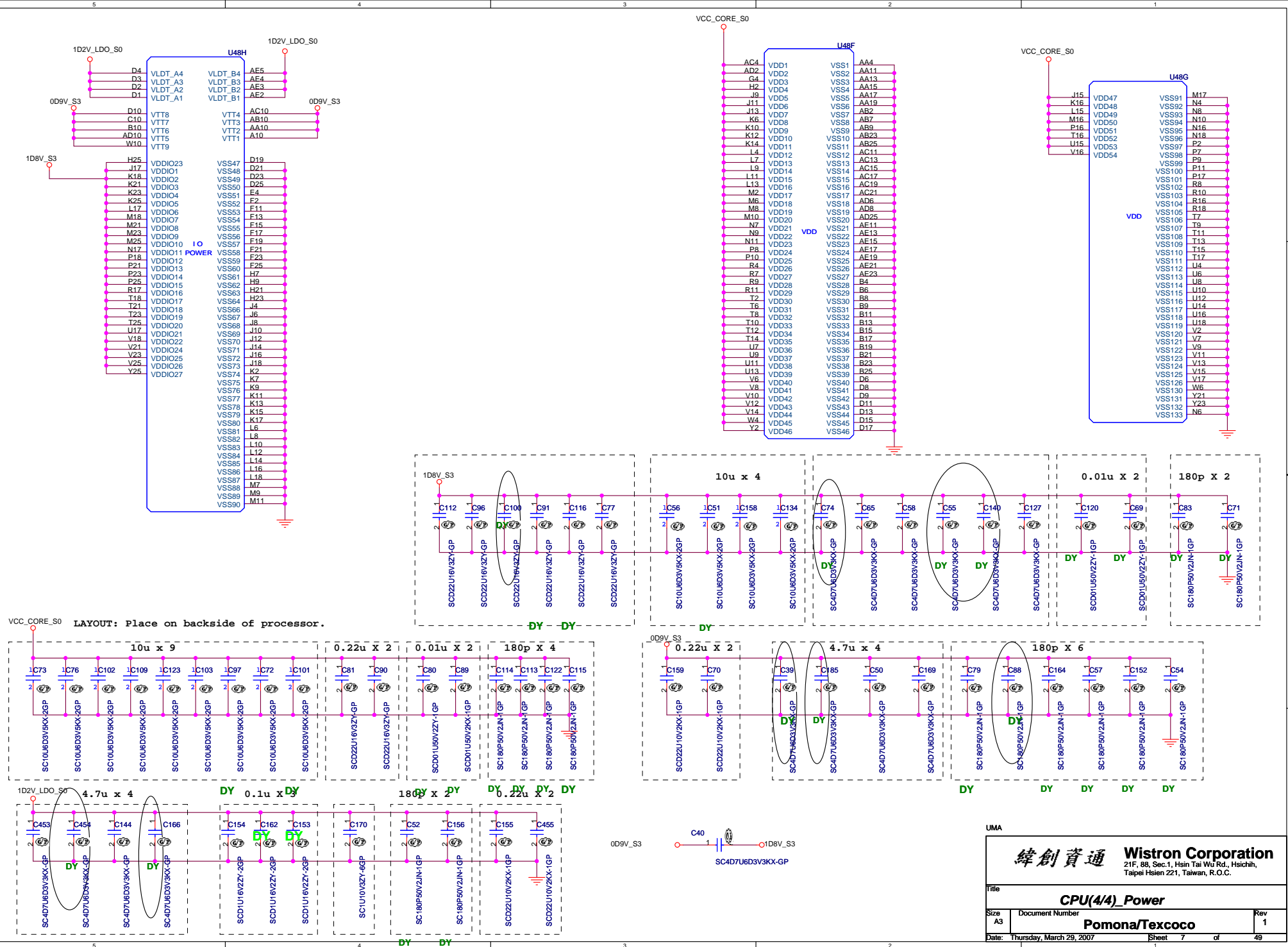


62.10055.111

UMA

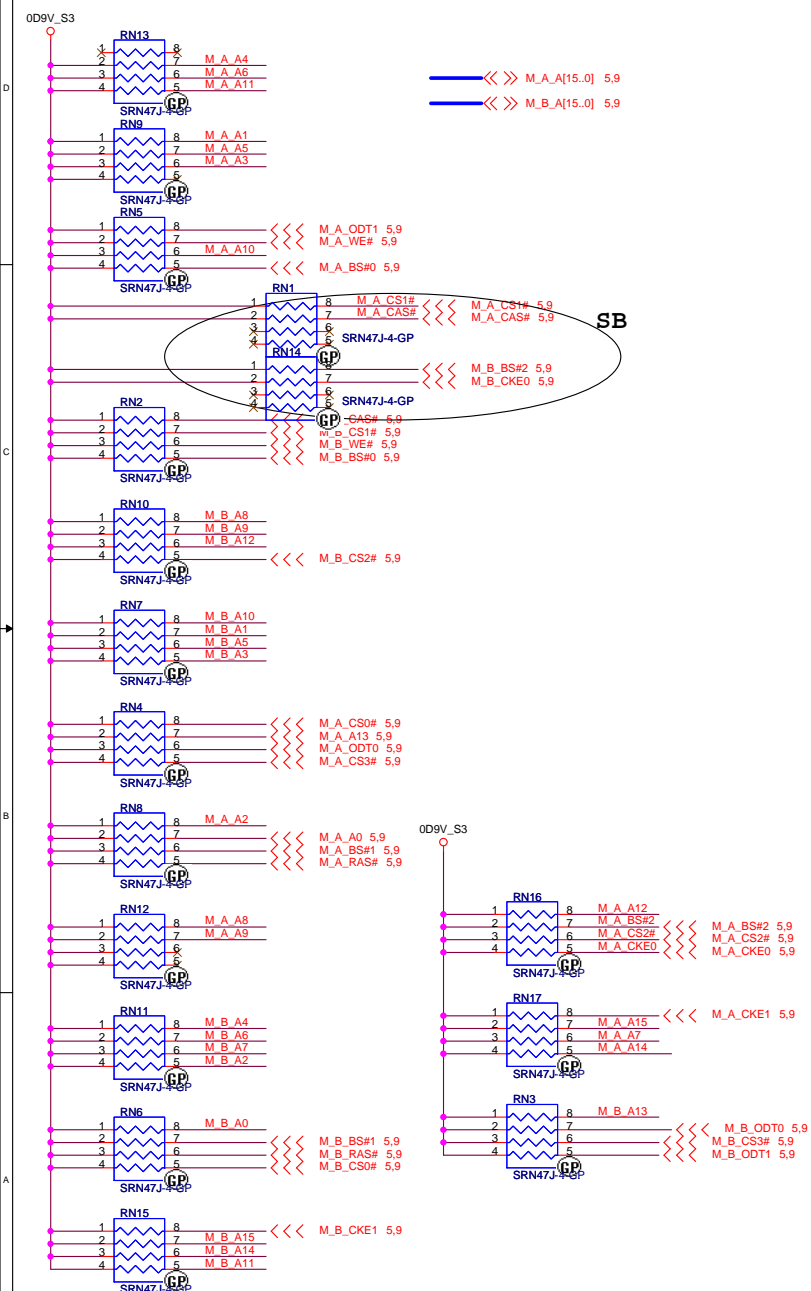
緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
CPU(1/4)_HyperTransport I/F			
Size	Document Number	Rev	
A3	Pomona/Textcoco	1	
Date: Thursday, March 29, 2007		Sheet 4 of 49	





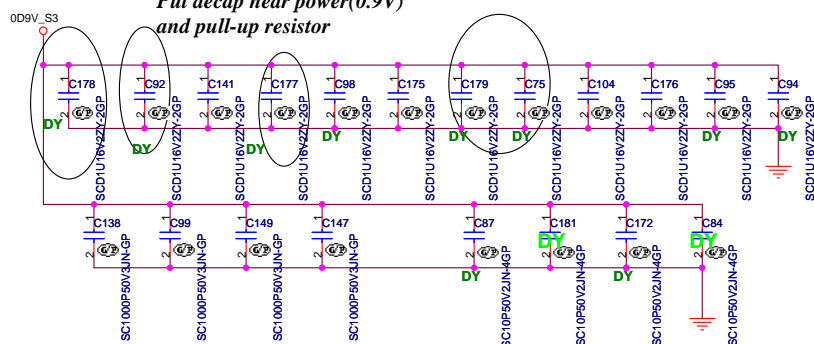
PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

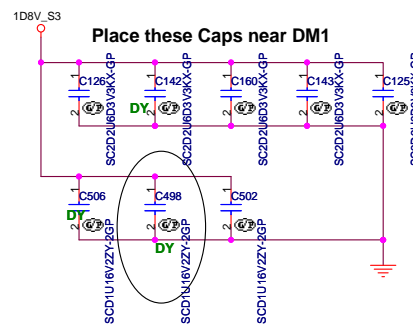


Decoupling Capacitor

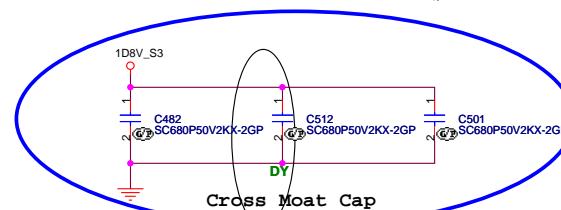
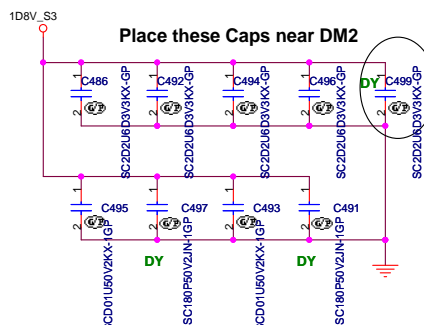
*Put decap near power(0.9V)
and pull-up resistor*



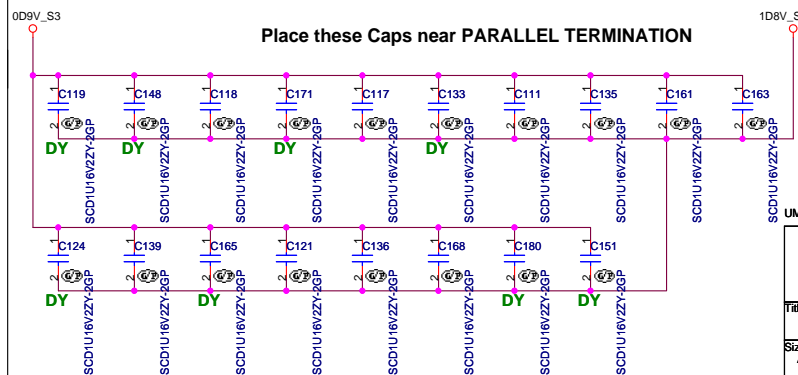
Place these Caps near DM1



Place these Caps near DM2



Place these Caps near PARALLEL TERMINATION



緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	DDR DAMPING & TERMINATION
-------	--------------------------------------

Size A3	Document Number Pomona/Textcoco	Rev 1
Date: Thursday, March 29, 2007	Sheet 8 of 49	

NORMAL TYPE

High 9.2mm

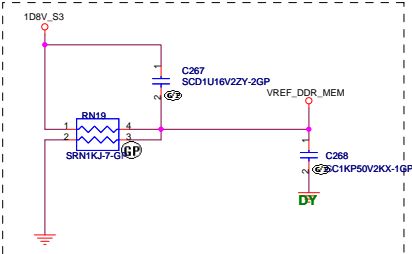
2ND = 62.10017.761

NORMAL TYPE

High 5.2mm

2ND = 62.10017.D91

VREF_DDR2_MEM



LAYOUT: Locate close to DIMM

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

DDR SO-DIMM SKT

Pomona/Textcoco

Thursday, March 29, 2007

Rev 1

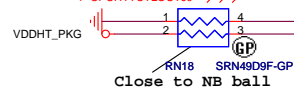
Sheet 9 of 48

CPU TO NB

4 CPUCADOUT[15..0] >>>
4 CPUCADOUTJ[15..0] >>>

CPUCADOUT15	R19	HT_RXCAD15P
CPUCADOUT15	R18	HT_RXCAD15N
CPUCADOUT14	R21	HT_RXCAD14P
CPUCADOUT14	R22	HT_RXCAD14N
CPUCADOUT13	U22	HT_RXCAD13P
CPUCADOUT13	U21	HT_RXCAD13N
CPUCADOUT12	U18	HT_RXCAD12P
CPUCADOUT12	U19	HT_RXCAD12N
CPUCADOUT11	W19	HT_RXCAD11P
CPUCADOUT11	W20	HT_RXCAD11N
CPUCADOUT10	AC21	HT_RXCAD10P
CPUCADOUT10	AB22	HT_RXCAD10N
CPUCADOUT9	AB20	HT_RXCAD9P
CPUCADOUT9	AA20	HT_RXCAD9N
CPUCADOUT8	AA19	HT_RXCAD8P
CPUCADOUT8	Y19	HT_RXCAD8N
CPUCADOUT7	T24	HT_RXCAD7P
CPUCADOUT7	R25	HT_RXCAD7N
CPUCADOUT6	U25	HT_RXCAD6P
CPUCADOUT6	U24	HT_RXCAD6N
CPUCADOUT5	V23	HT_RXCAD5P
CPUCADOUT5	U23	HT_RXCAD5N
CPUCADOUT4	V24	HT_RXCAD4P
CPUCADOUT4	V25	HT_RXCAD4N
CPUCADOUT3	AA24	HT_RXCAD3P
CPUCADOUT3	AA25	HT_RXCAD3N
CPUCADOUT2	AB23	HT_RXCAD2P
CPUCADOUT2	AA23	HT_RXCAD2N
CPUCADOUT1	AB24	HT_RXCAD1P
CPUCADOUT1	AB25	HT_RXCAD1N
CPUCADOUT0	AC24	HT_RXCAD0P
CPUCADOUT0	AC25	HT_RXCAD0N

4 CPUHTTCLKOUT1	>>>	CPUHTTCLKOUT1	W21	HT_RXCLK1P
4 CPUHTTCLKOUTJ1	>>>	CPUHTTCLKOUTJ1	W22	HT_RXCLK1N
4 CPUHTTCLKOUT0	>>>	CPUHTTCLKOUT0	Y24	HT_RXCLK0P
4 CPUHTTCLKOUTJ0	>>>	CPUHTTCLKOUTJ0	W25	HT_RXCLK0N
4 CPUHTTCTLOUT0	>>>	CPUHTTCTLOUT0	P24	HT_RXCTLP
4 CPUHTTCTLOUTJ0	>>>	CPUHTTCTLOUTJ0	P25	HT_RXCTLN



U51A 1 of 5

HYPER TRANSPORT CPU
I/F

HT_TXCAD15P	HT_TXCAD15N
HT_TXCAD14P	HT_TXCAD14N
HT_TXCAD13P	HT_TXCAD13N
HT_TXCAD12P	HT_TXCAD12N
HT_TXCAD11P	HT_TXCAD11N
HT_TXCAD10P	HT_TXCAD10N
HT_TXCAD9P	HT_TXCAD9N
HT_TXCAD8P	HT_TXCAD8N
HT_TXCAD7P	HT_TXCAD7N
HT_TXCAD6P	HT_TXCAD6N
HT_TXCAD5P	HT_TXCAD5N
HT_TXCAD4P	HT_TXCAD4N
HT_TXCAD3P	HT_TXCAD3N
HT_TXCAD2P	HT_TXCAD2N
HT_TXCAD1P	HT_TXCAD1N
HT_TXCAD0P	HT_TXCAD0N
HT_TXCLK1P	HT_TXCLK1N
HT_TXCLK0P	HT_TXCLK0N
HT_TXCTLP	HT_TXCTLN
HT_TXCALP	HT_TXCALN

RS690M-GP

71.RS690.M01

NB TO CPU

>>> NB0CADOUT[15..0] 4
>>> NB0CADOUTJ[15..0] 4

P21	NB0CADOUT15
P22	NB0CADOUT15
P18	NB0CADOUT14
P19	NB0CADOUT14
M22	NB0CADOUT13
M21	NB0CADOUT13
M18	NB0CADOUT12
M19	NB0CADOUT12
L18	NB0CADOUT11
L19	NB0CADOUT11
G22	NB0CADOUT10
G21	NB0CADOUT10
J20	NB0CADOUT9
J21	NB0CADOUT9
F21	NB0CADOUT8
F22	NB0CADOUT8
N24	NB0CADOUT7
N25	NB0CADOUT7
L25	NB0CADOUT6
M24	NB0CADOUT6
K25	NB0CADOUT5
K24	NB0CADOUT5
J23	NB0CADOUT4
J23	NB0CADOUT4
G25	NB0CADOUT3
H24	NB0CADOUT3
E25	NB0CADOUT2
F24	NB0CADOUT2
E23	NB0CADOUT1
F23	NB0CADOUT1
E24	NB0CADOUT0
E25	NB0CADOUT0

L21	NB0HTTCLKOUT1	>>>	NB0HTTCLKOUT1 4
L22	NB0HTTCLKOUTJ1	>>>	NB0HTTCLKOUTJ1 4
J24	NB0HTTCLKOUT0	>>>	NB0HTTCLKOUT0 4
J25	NB0HTTCLKOUTJ0	>>>	NB0HTTCLKOUTJ0 4
N23	NB0HTTCTLOUT	>>>	NB0HTTCTLOUT 4
P23	NB0HTTCTLOUTJ	>>>	NB0HTTCTLOUTJ 4
C25	HT_TXCALP		
D24	HT_TXCALN		

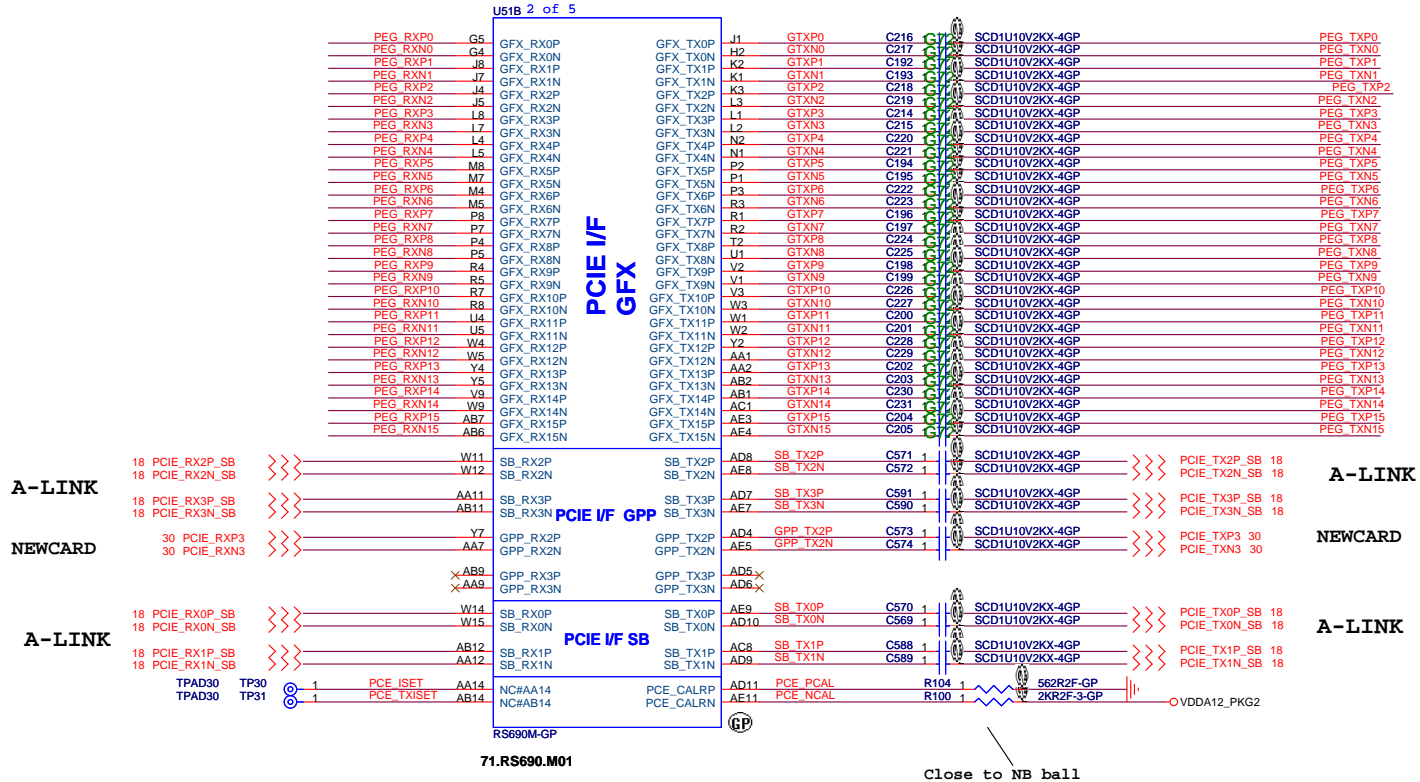
Close to NB ball

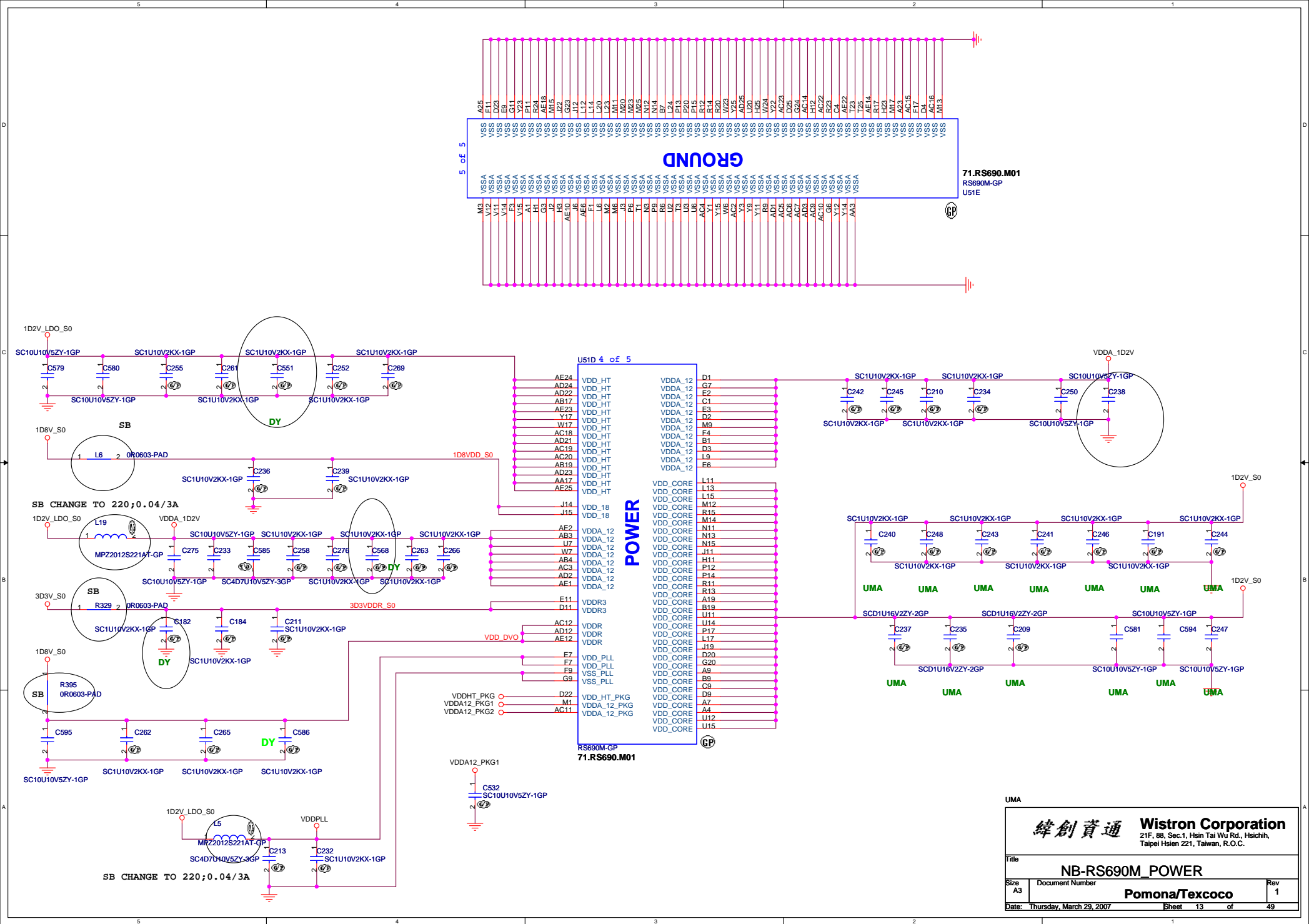
UMA

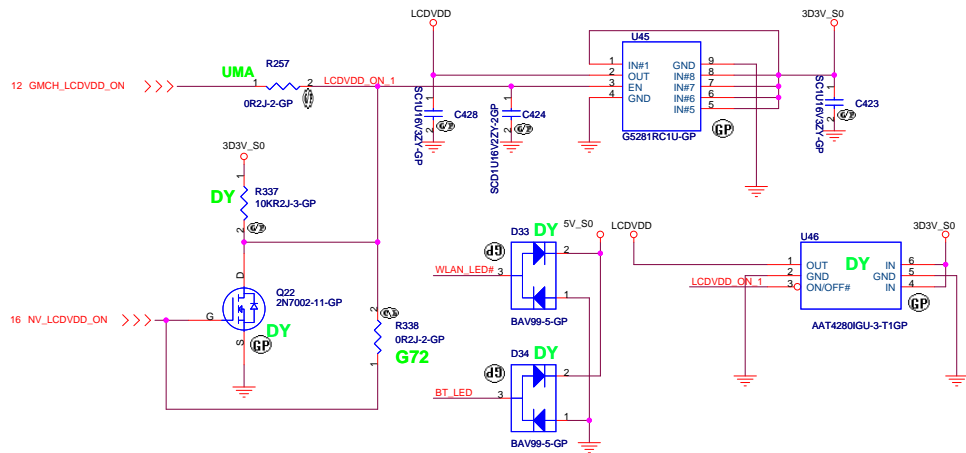
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
NB-RS690M HT			
Size	Document Number	Rev	
A3	Pomona/Texcoco	1	
Date: Thursday, March 29, 2007		Sheet	10 of 49

16 PEG_RXN[15..0] >>>
16 PEG_RXP[15..0] >>>

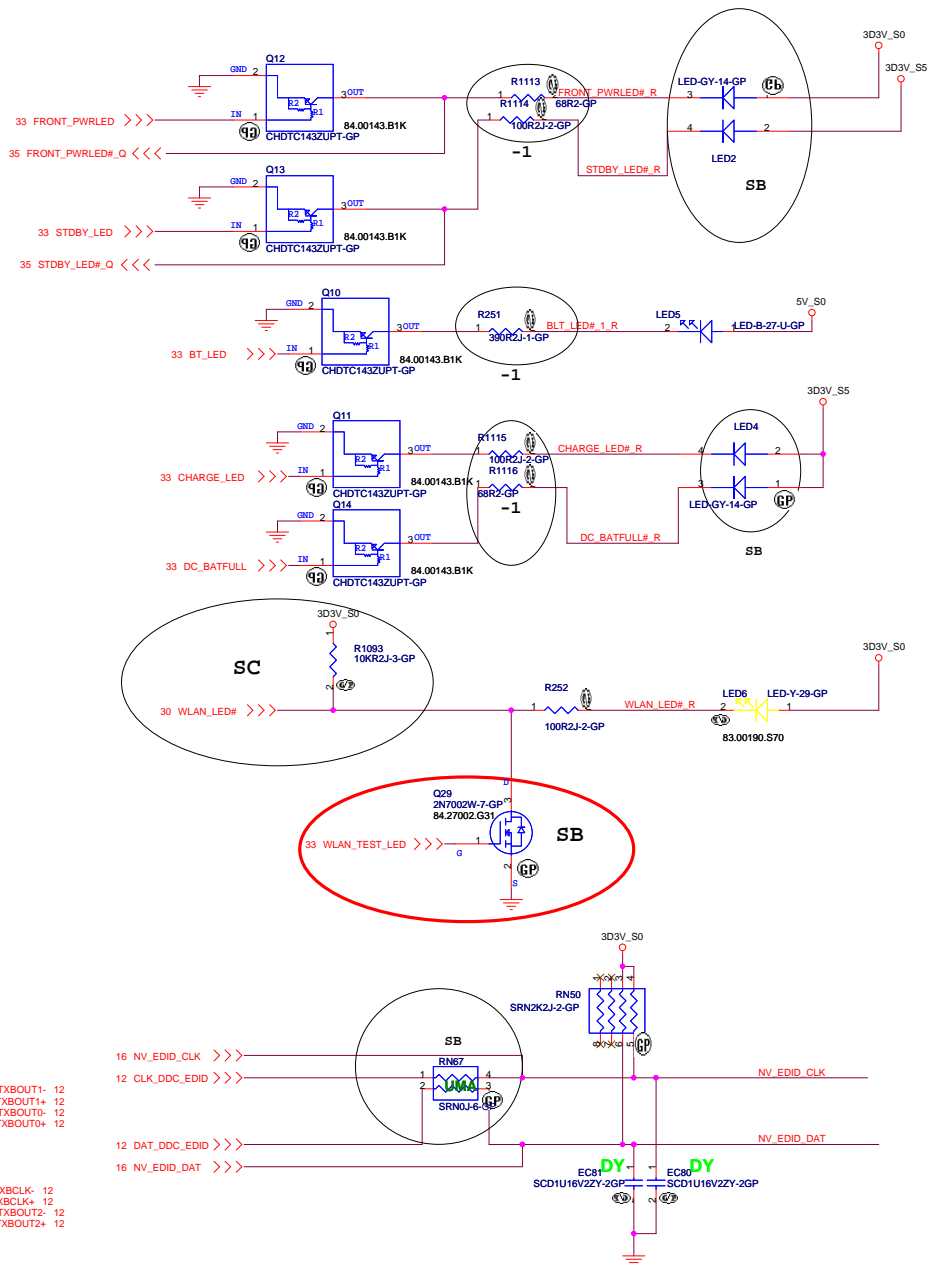
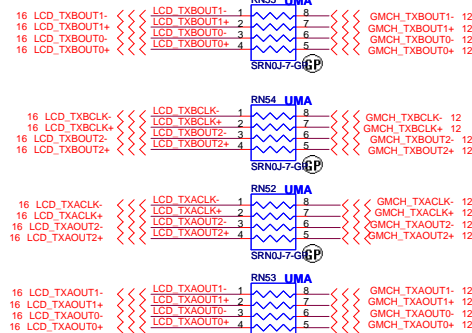
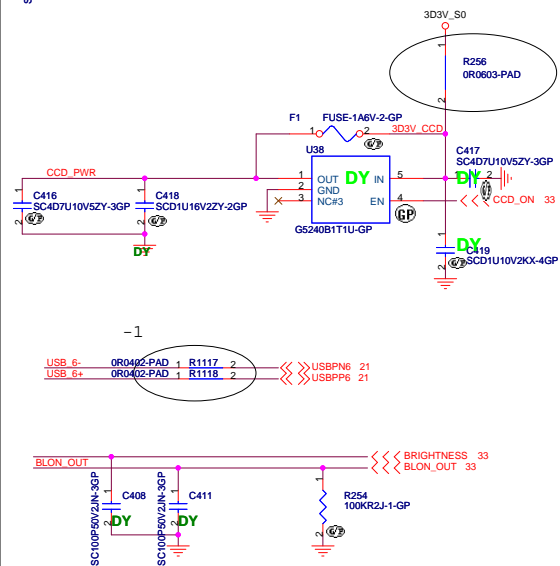
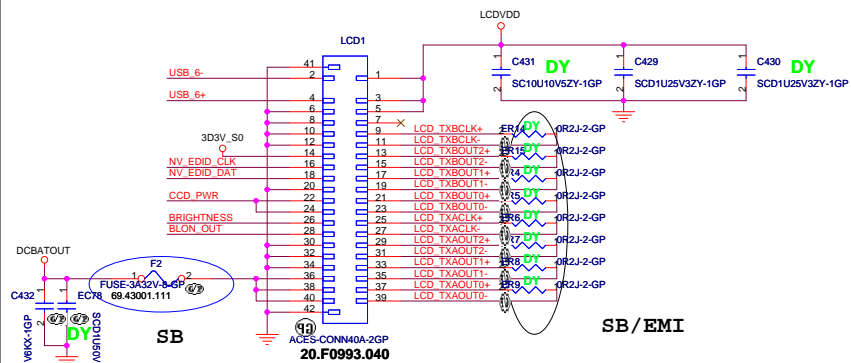
>>> PEG_TXN[15..0] 16
>>> PEG_TXP[15..0] 16



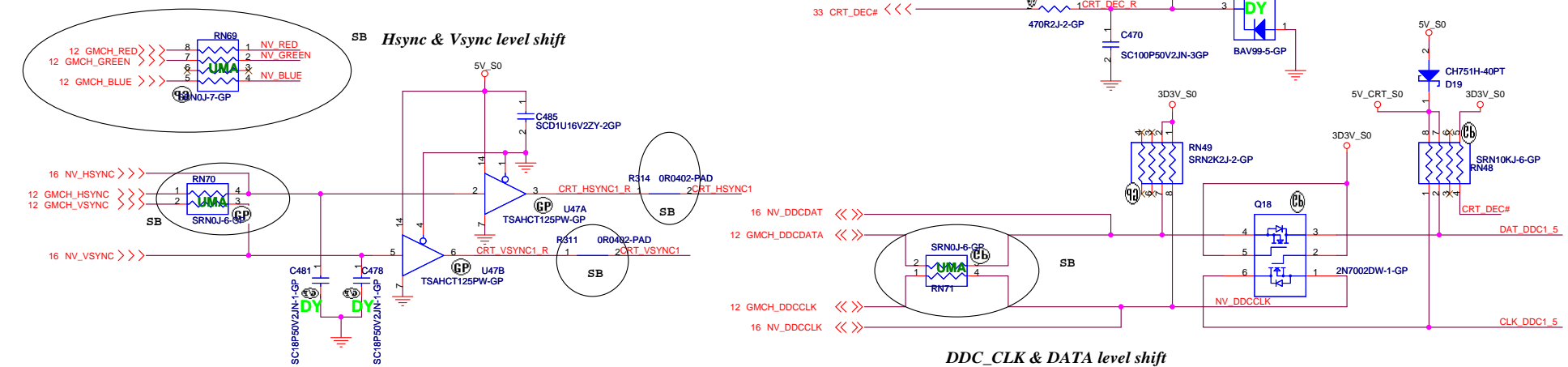
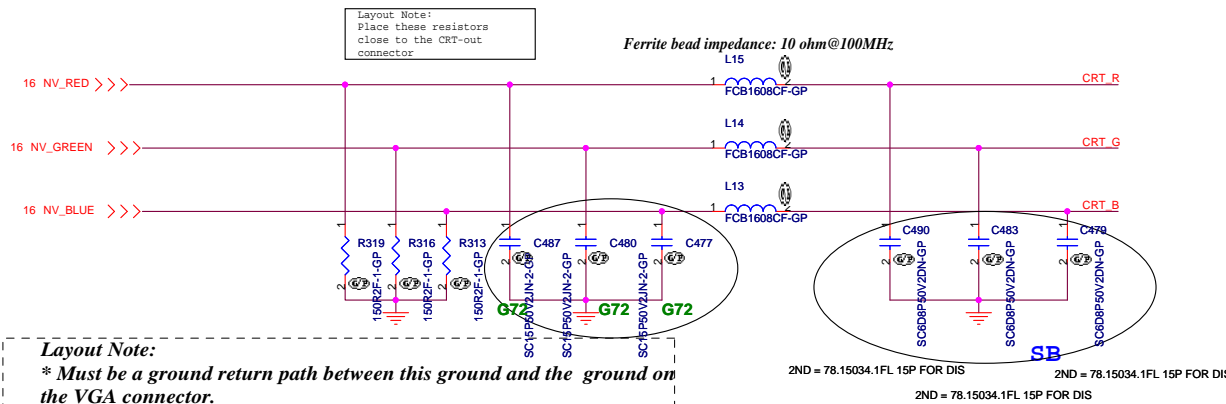




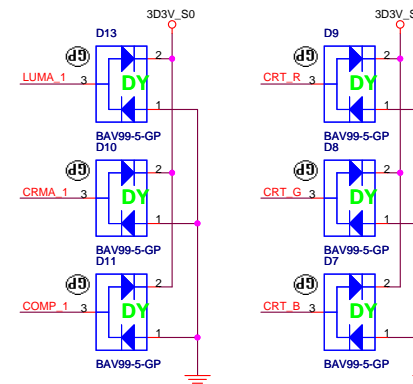
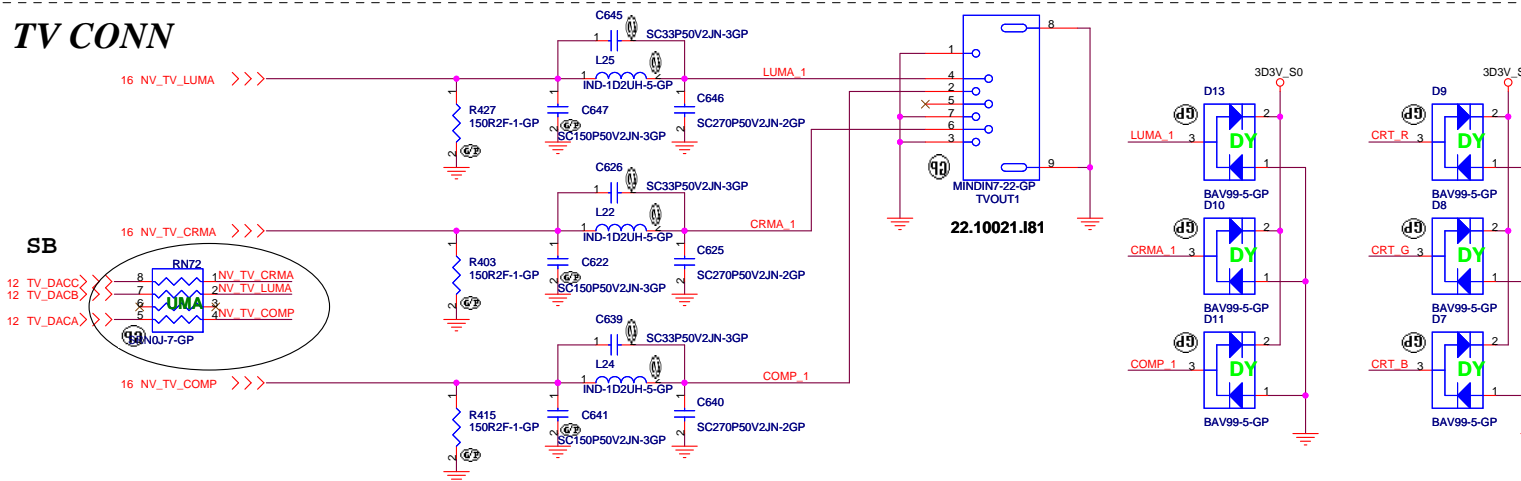
LCD/INVERTER CONN



CRT I/F & CONNECTOR



TV CONN



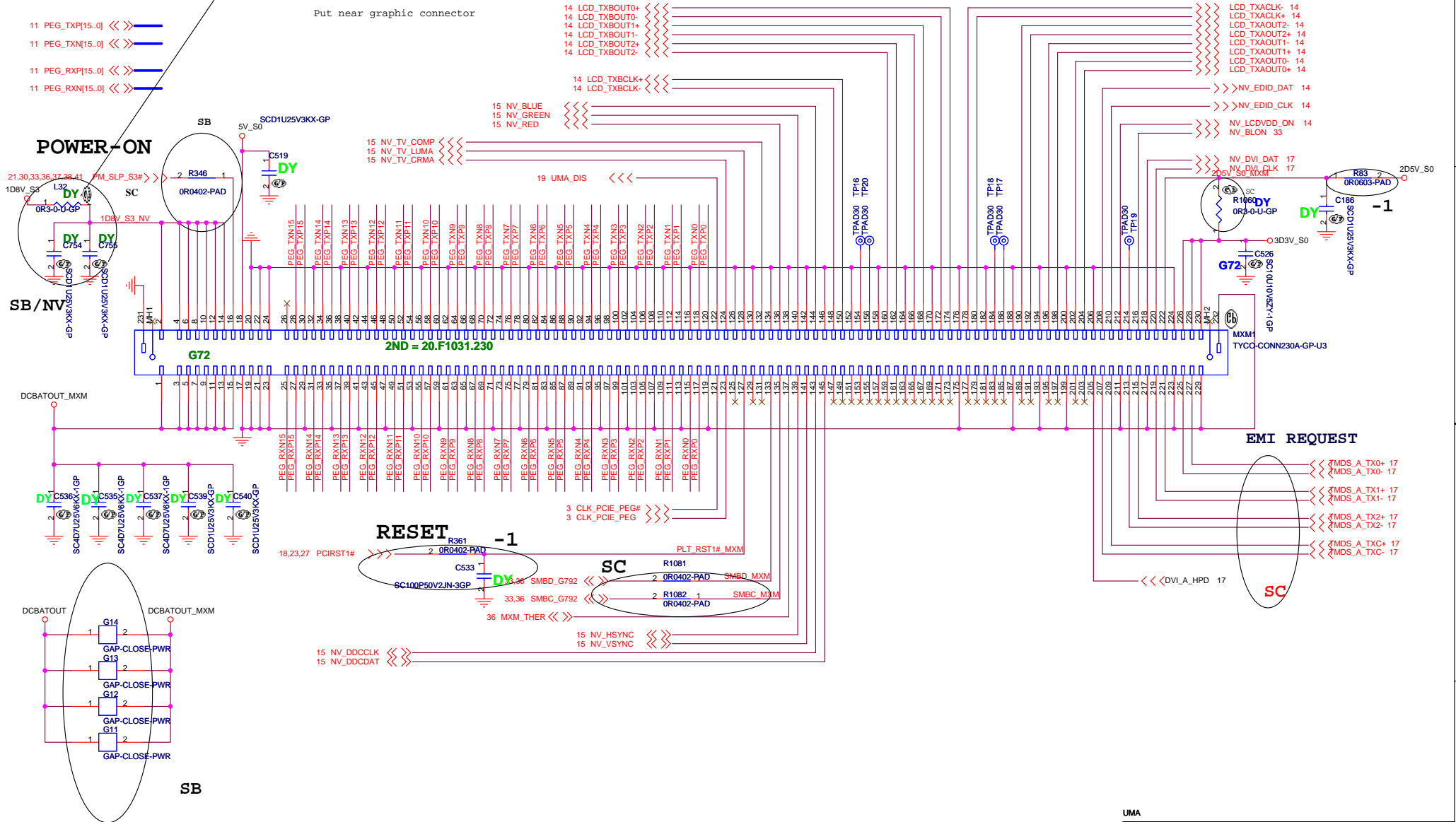
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
CRT/TV Connector			
Size	Document Number		Rev
	Pomona/Textcoco		1
Date:	Thursday, March 29, 2007	Sheet 15 of	49

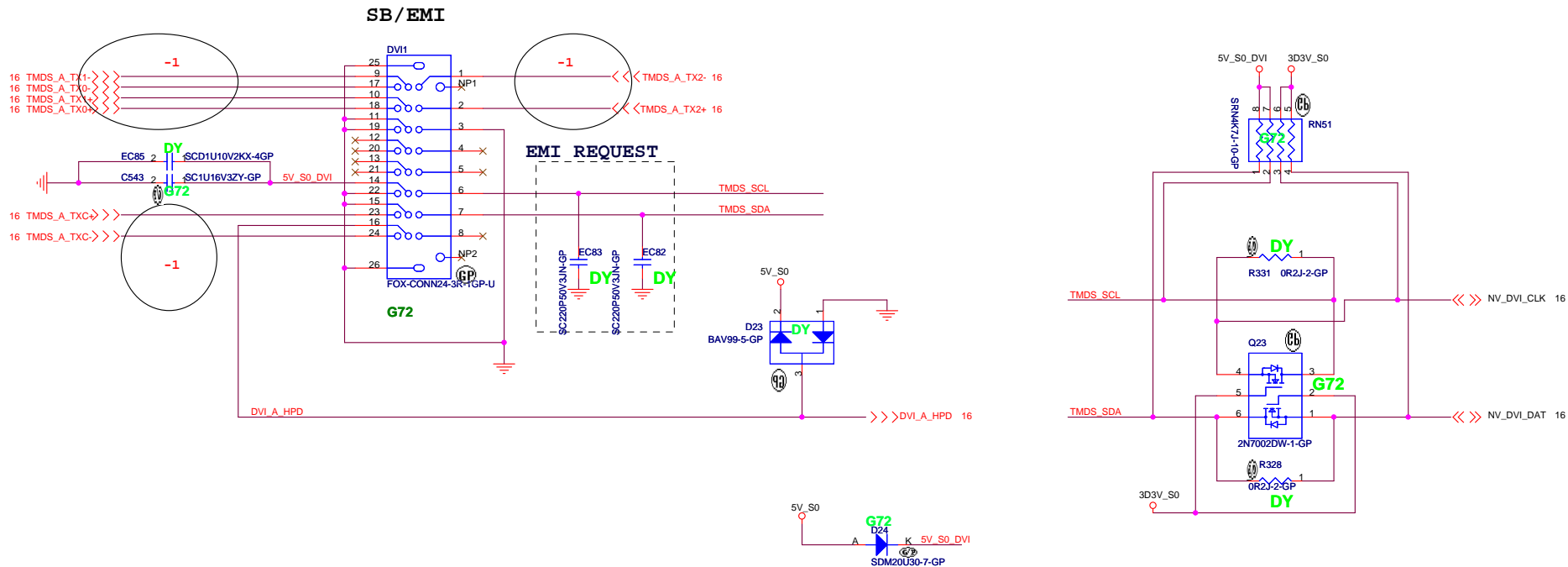
ENG MUST STUFF FOR ATI

Put near graphic connector

NV SMBus
A(pin143&145) : VGA(CRT) / DOCK
B(pin218&220) : DVI
C(pin208&210) : HDMI / TPI / LVDS



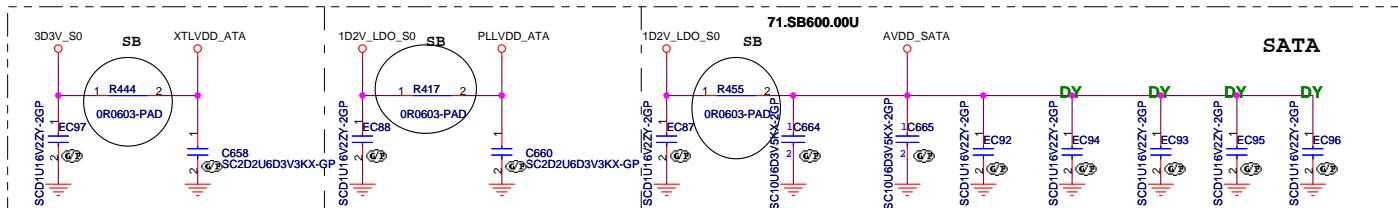
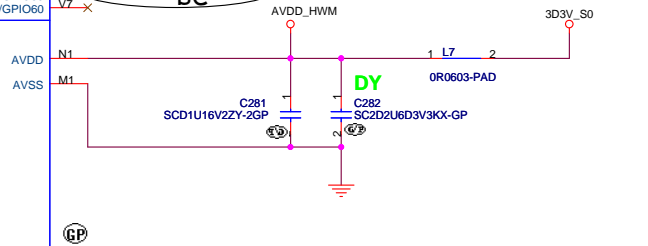
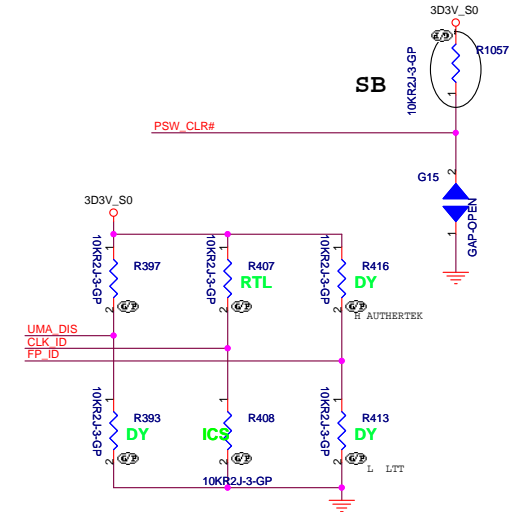
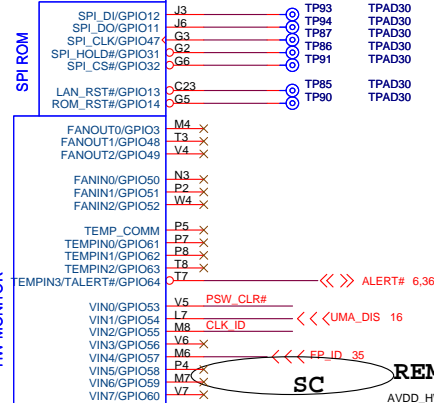
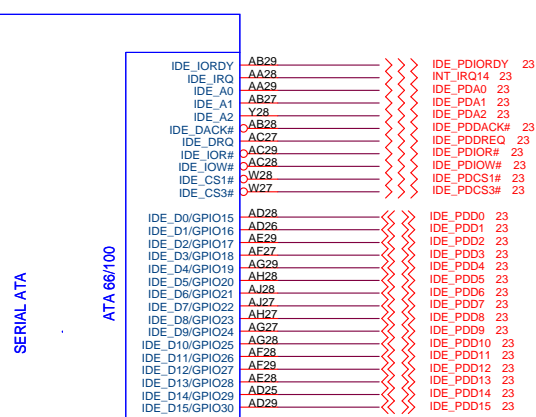
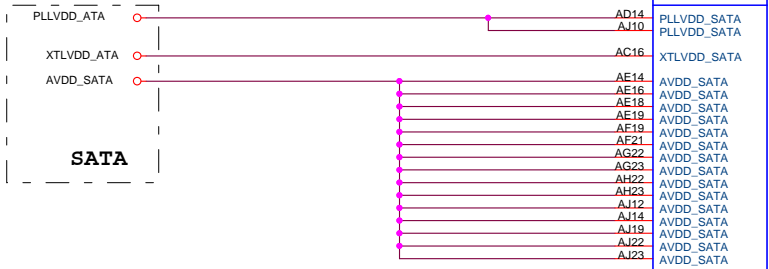
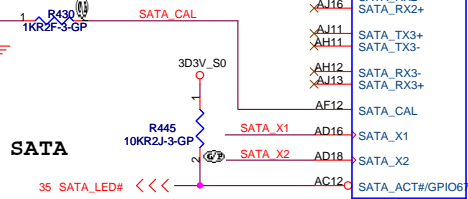
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
Graphic MXM CONN		
Size A3	Document Number Pomona/Texcoco	Rev 1
Date: Thursday, March 29, 2007	Sheet 16 of 49	

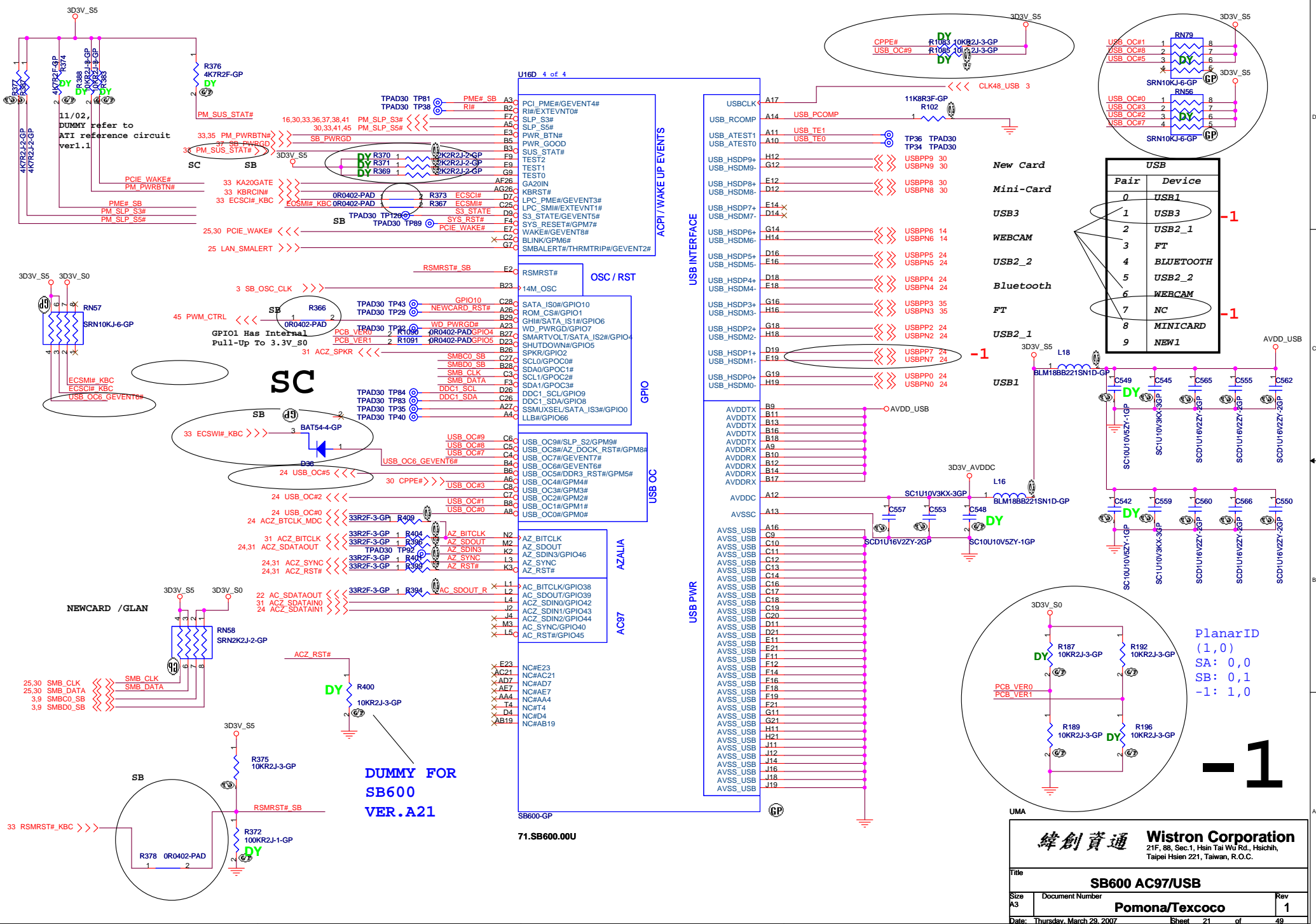


UMA

緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
DVI CONNECTOR			
Size A3	Document Number Pomona/Textcoco		Rev 1
Date: Thursday, March 29, 2007		Sheet 17 of 49	

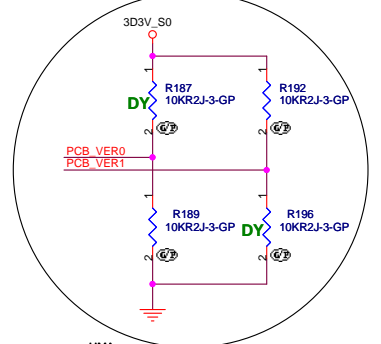


[illegible]



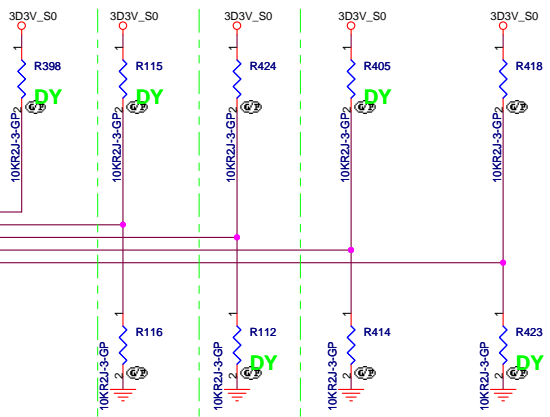
USB	
Pair	Device
0	USB1
1	USB3
2	USB2_1
3	FT
4	BLUETOOTH
5	USB2_2
6	WEBCAM
7	NC
8	MINICARD
9	NEW1

New Card
Mini-Card
USB3
WEBCAM
USB2_2
Bluetooth
FT
USB2_1



PCI_CLK4
PCI_CLK6
PCI_CLK0
PCI_CLK1

21 AC_SDATAOUT
18.33 PCLK_KBC
18 CLK33 LPCROM
18.33 PCI_CLK0
18.27 PCLK_PCM

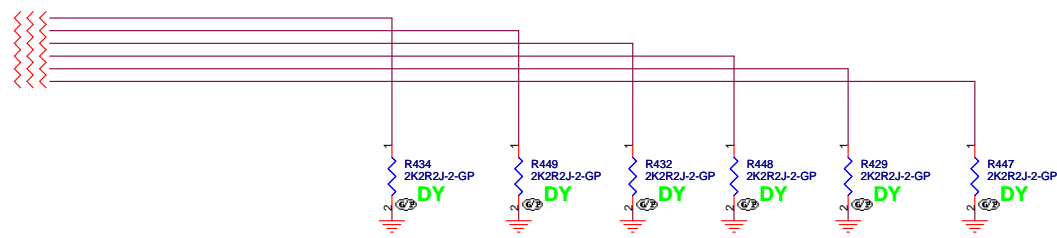


REQUIRED SYSTEM STRAPS

SB600					
	AC_SDOUT	PCI_CLK4	PCI_CLK6	PCI_CLK0	PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	USE INT. PLL48	CPU IF=K8 DEFAULT	ROM TYPE: H, H = PCI ROM H, L = SPI ROM L, H = LPC ROM L, L = FWH ROM	DEFAULT
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	USE EXT. 48MHZ DEFAULT	CPU IF=P4		

SB600 HAS 15K INTERNAL PU FOR PCI_AD[23..28]

18.27 PCI_AD28
18.27 PCI_AD27
18.27 PCI_AD26
18.27 PCI_AD25
18.27 PCI_AD24
18.27 PCI_AD23



DEBUG STRAPS

	PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
STRAP HIGH	RESERVED	RESERVED	RESERVED	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	BOOT FAIL TIMER DISABLE DEFAULT
STRAP LOW				USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOT FAIL TIMER ENABLE

UMA

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title

SB600 STRAPPING PIN

Size

A3

Document Number

Pomona/Texcoco

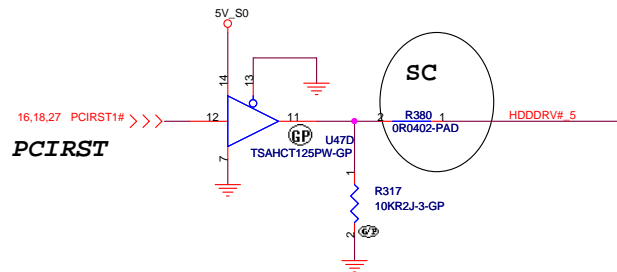
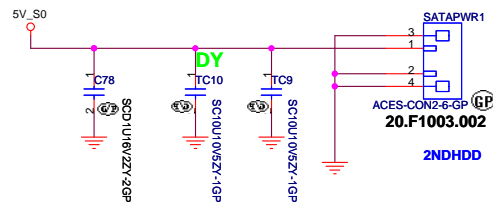
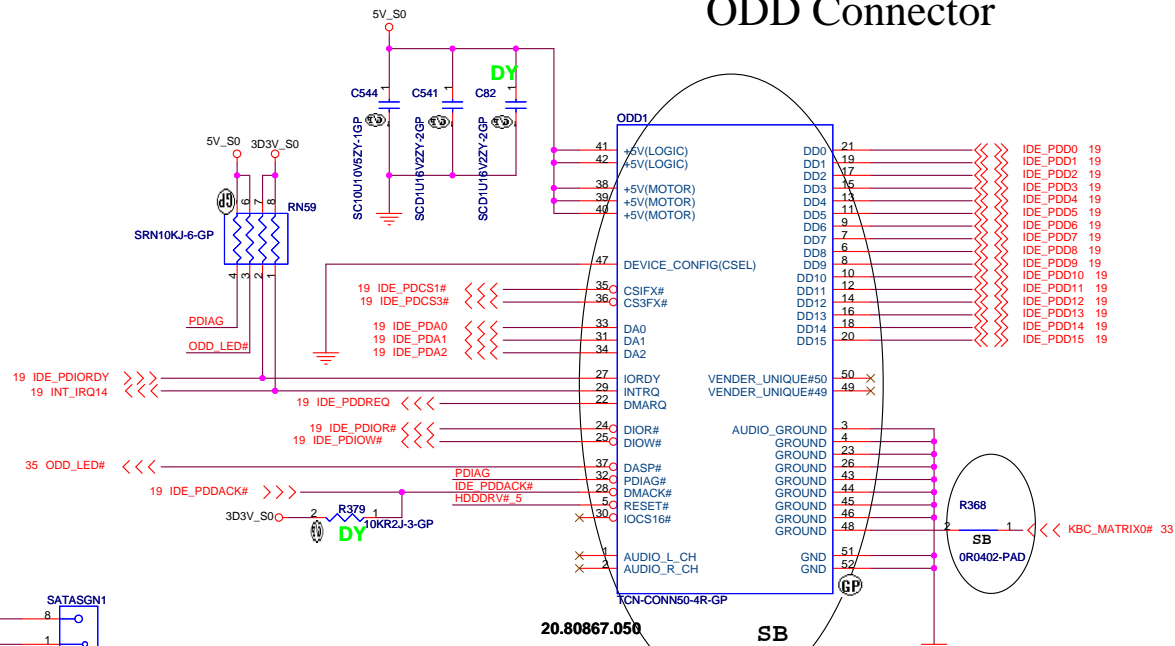
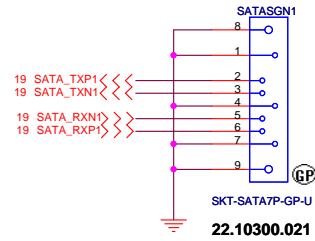
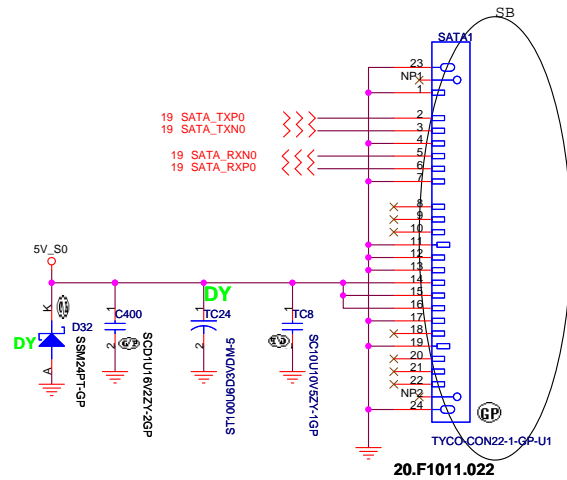
Rev

1

Date: Thursday, March 29, 2007

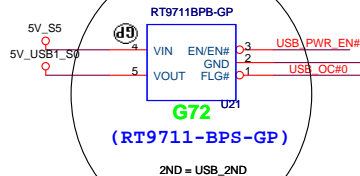
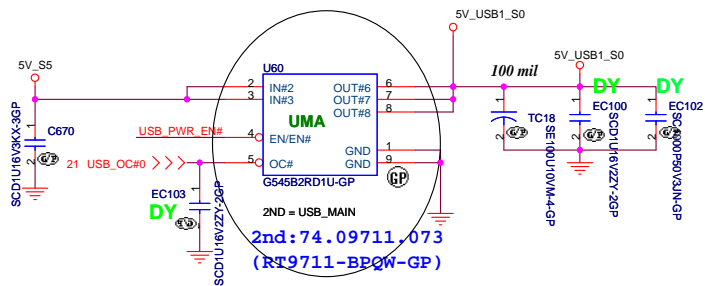
Sheet 22 of 49

SATA HD Connector

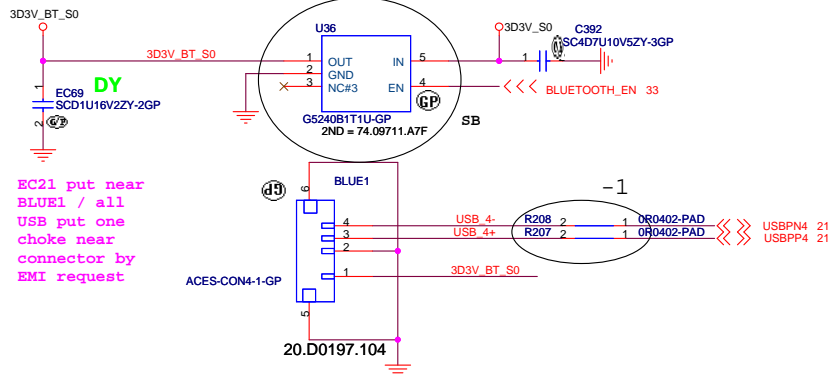


UMA

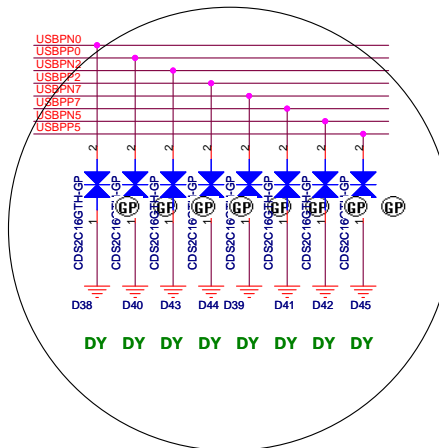
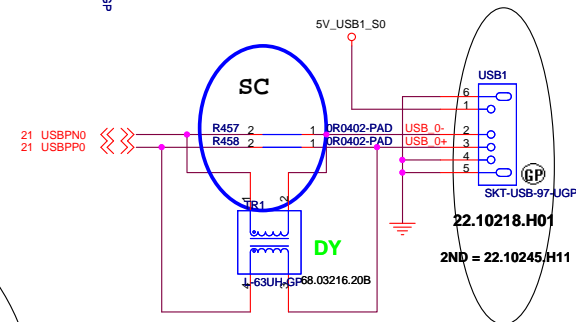
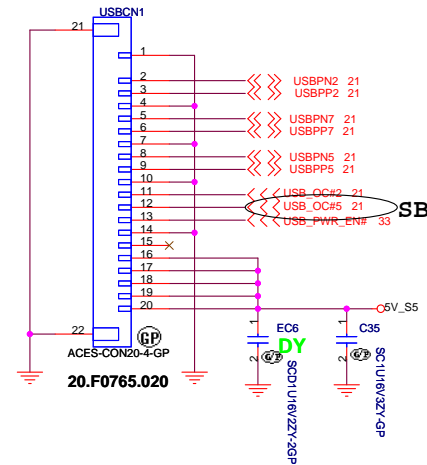
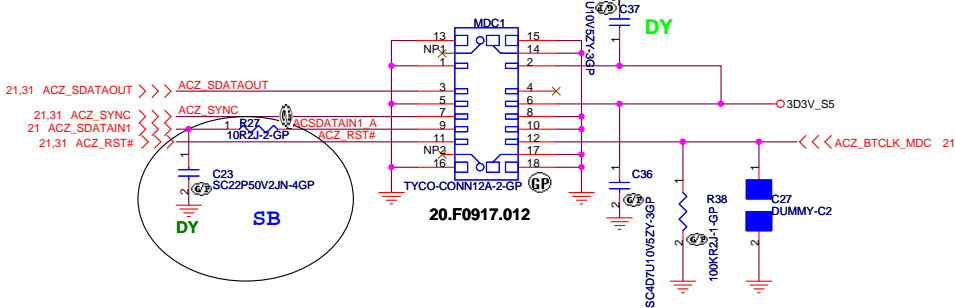
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
Size Document Number	
Date: Thursday, March 29, 2007	
Sheet 23 of 49	
HDD and CDROM Pomona/Textcoco	
Rev 1	



BLUETOOTH MODULE

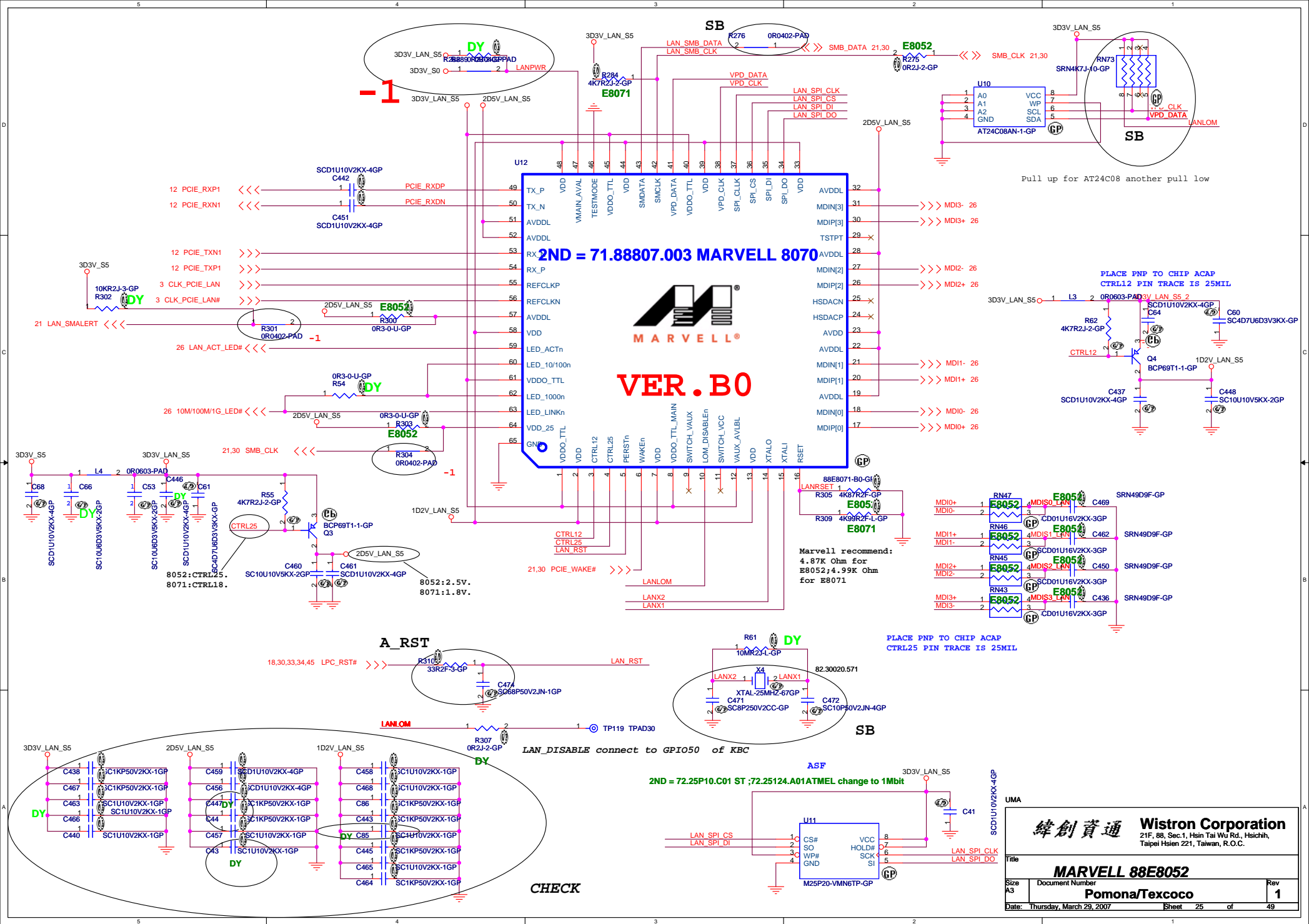


MDC 1.5 CONN

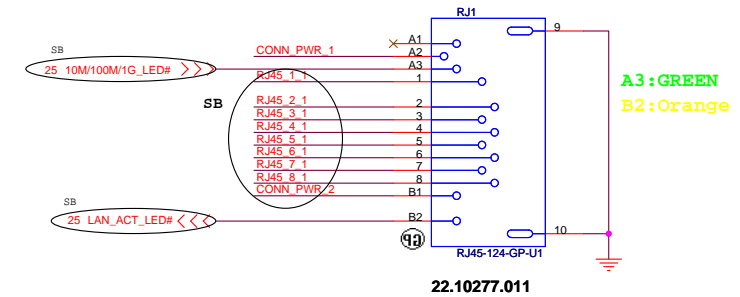


SC

UMA			
緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
USB / MDC / BLUETOOTH			
Size	Document Number		Rev
	Pomona/Textcoco		1
Date:	Thursday, March 29, 2007	Sheet 24	of 49



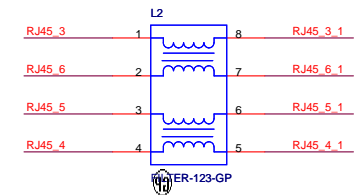
LAN Connector



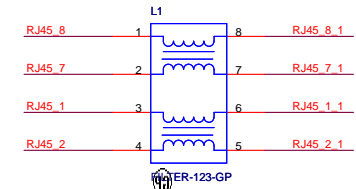
LAN Link: Green(A3), behavior is the same for 10/100/1000 bits

LAN Data: Yellow(B2), when LAN is transferring data.

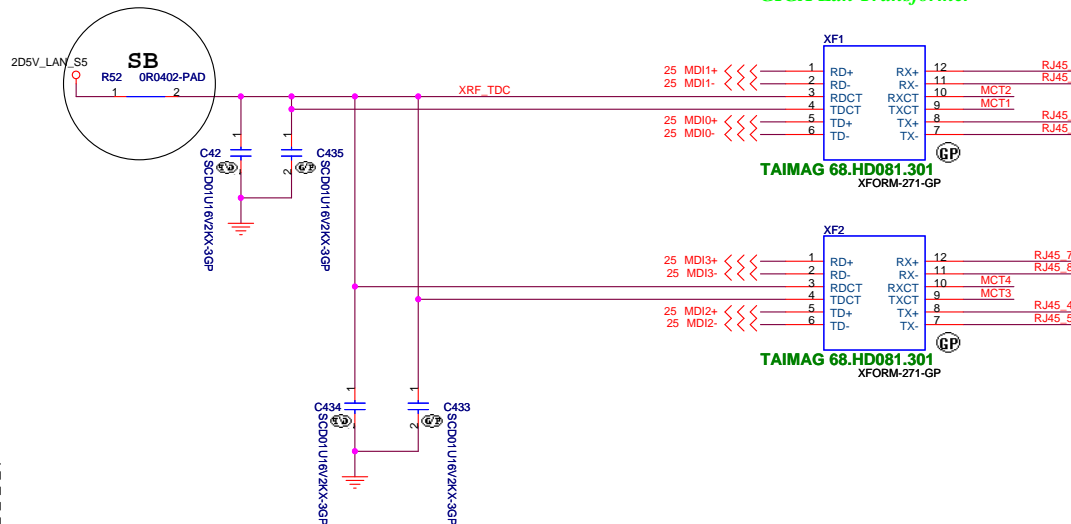
For EMI



-1



SC CHANGE 69.10106.021 TO 69.10106.011



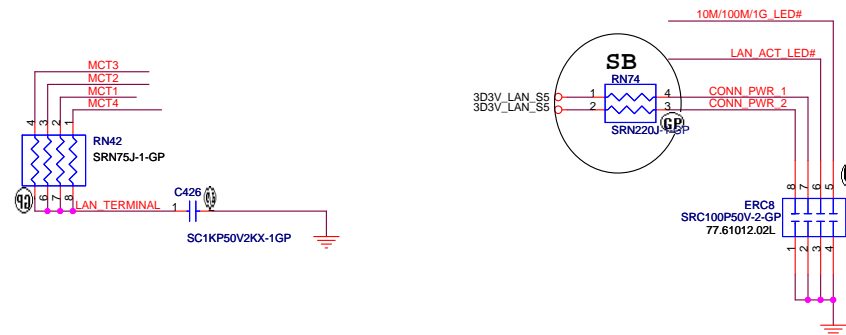
- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.

RJ11 signal must leave the other signal or power plane 100mil.

DOC_TIP,DOC_RING,TIP,RING:

W/S: 10/100 @ Surface layers
10/20 @ Inner layers

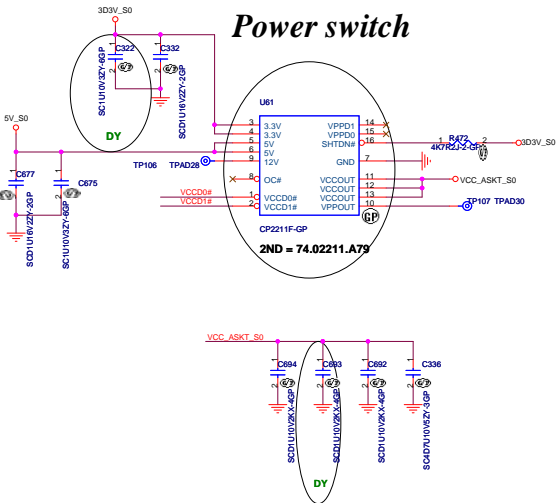
10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6

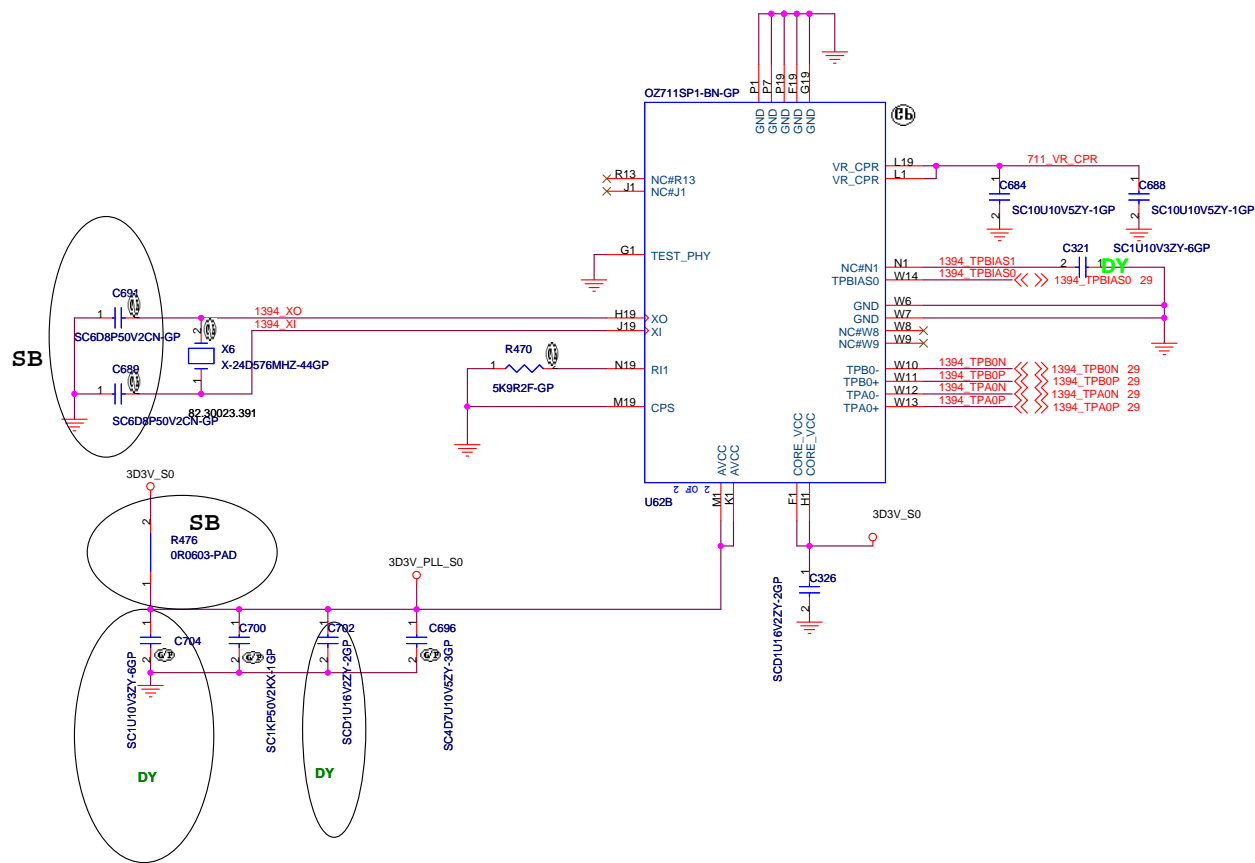


UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN Connector
Size: A3 Document Number: Pomona/Textcoco Rev: 1
Date: Thursday, March 29, 2007 Sheet: 26 of 49





UMA

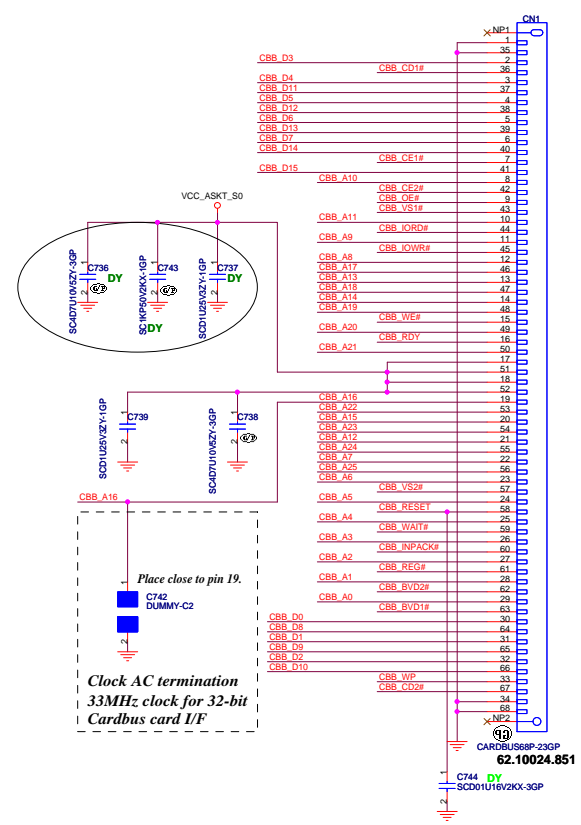
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **OZ711SP1 (2 of 2)**

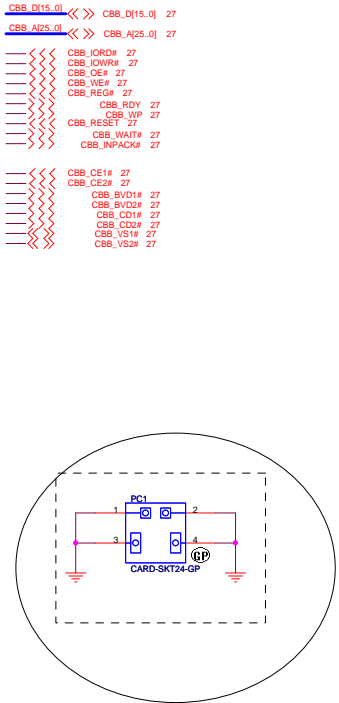
Size Document Number **Pomona/Textcoco** Rev **1**

Date: Thursday, March 29, 2007 Sheet 28 of 49

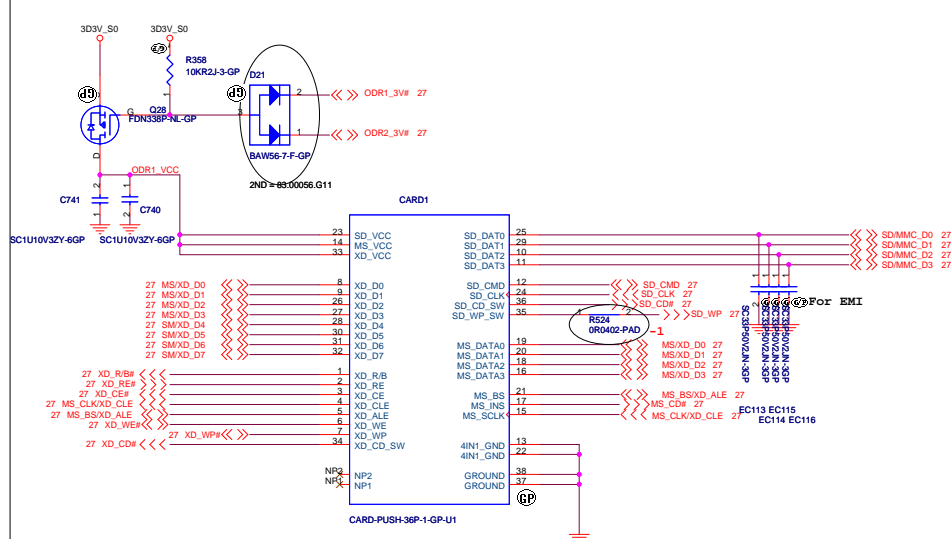
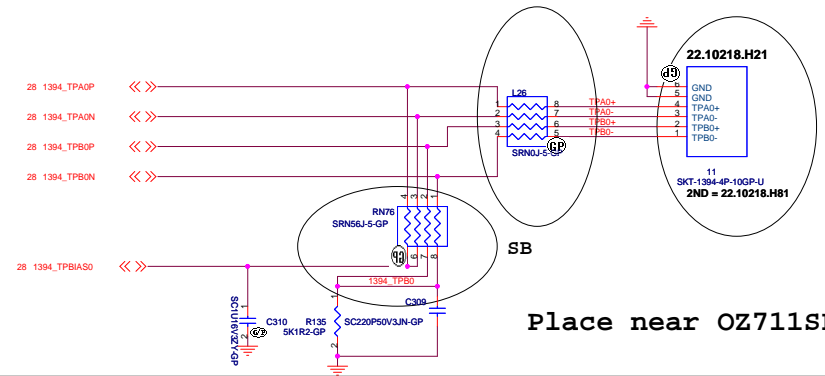
PCMCIA Socket



Cardbus I/F

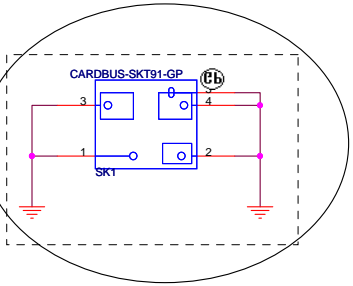


1394 Connector



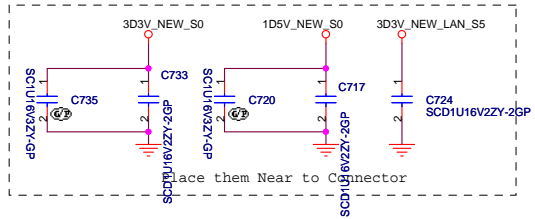
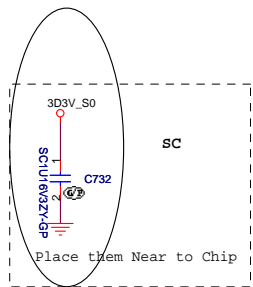
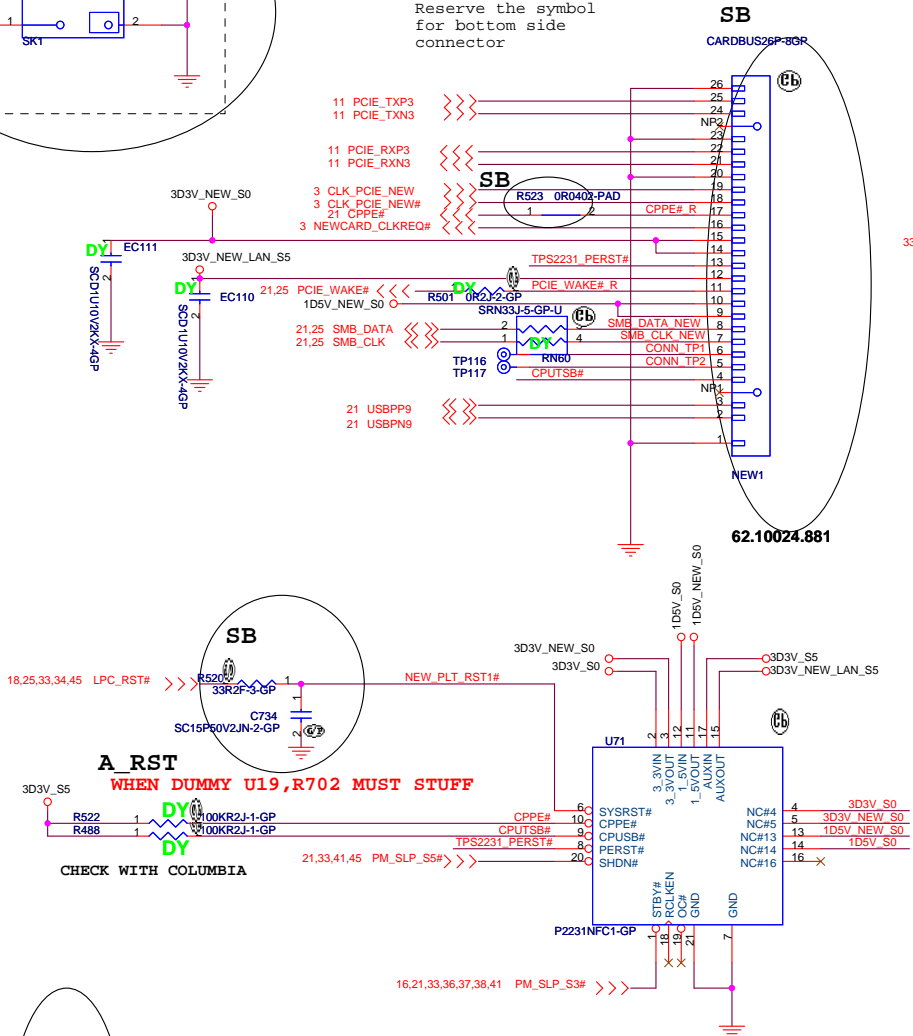
XD
MS / MS PRO
SD / SD IO / MMC

Mini Card Connector

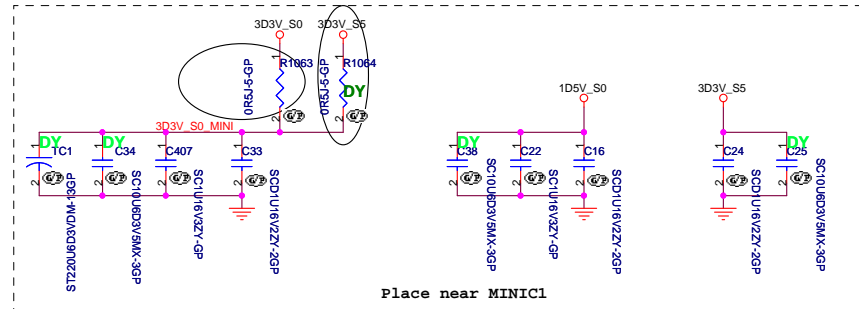
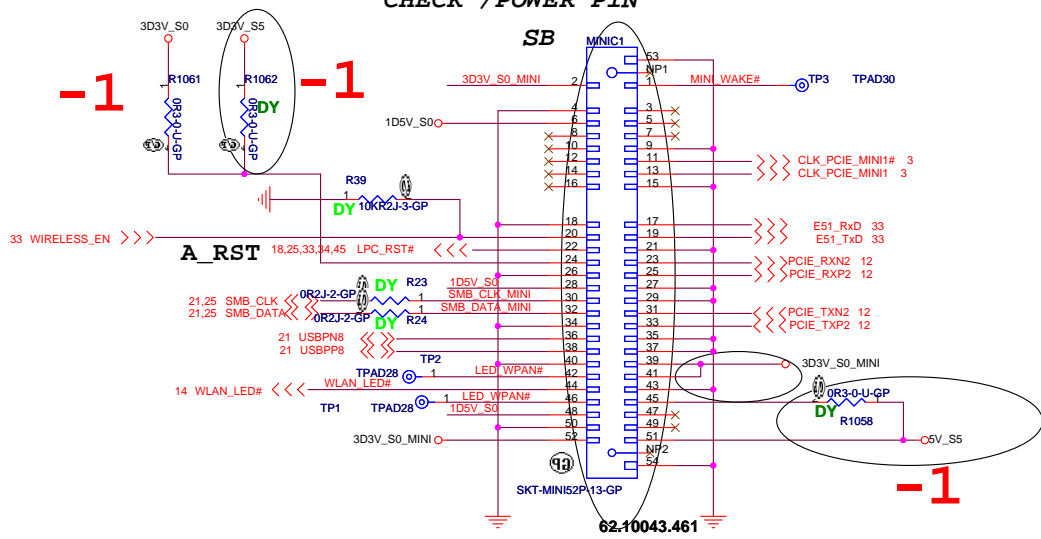


NEWCARD Connector

Reserve the symbol
for bottom side
connector



CHECK /POWER PIN



UMA

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

MINI CARD / NEW CARD

Size

Document Number

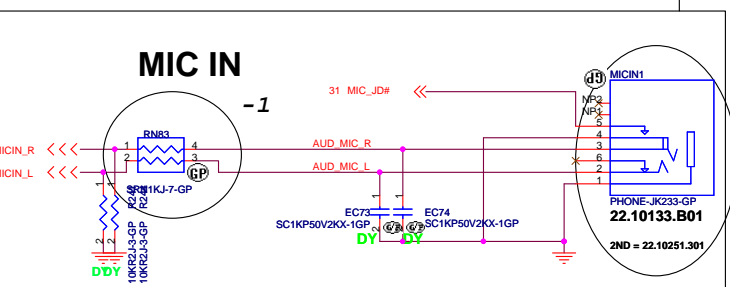
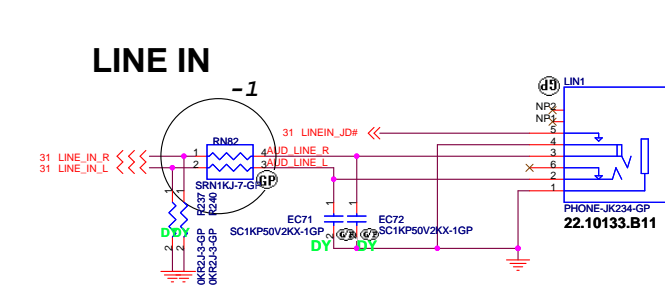
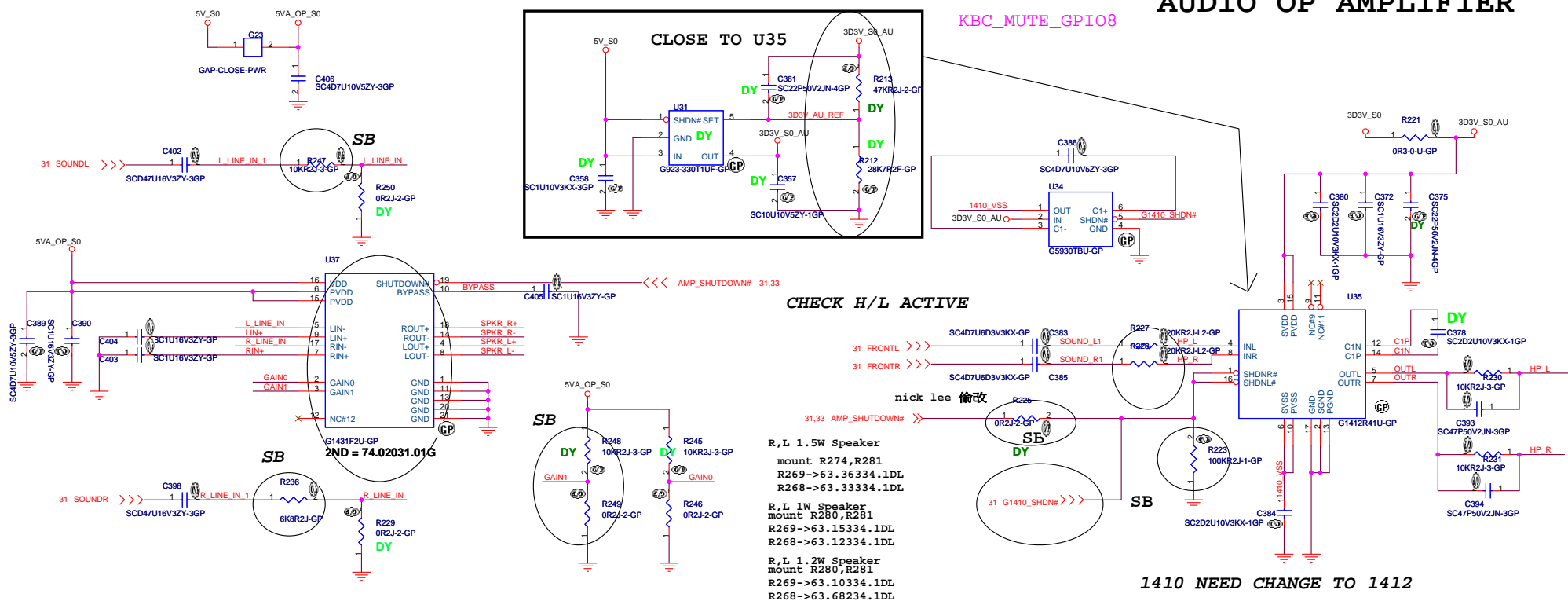
Pomona/Texcoco

Date: Thursday, March 29, 2007

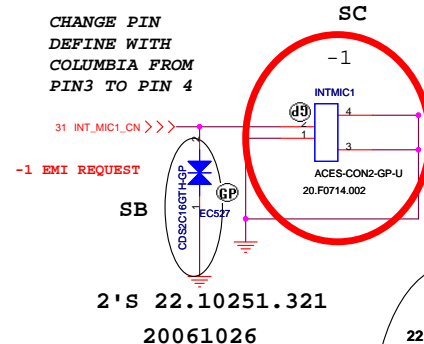
Sheet 30 of 49

Rev

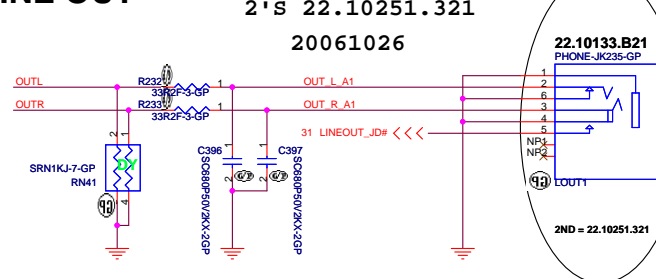
AUDIO OP AMPLIFIER



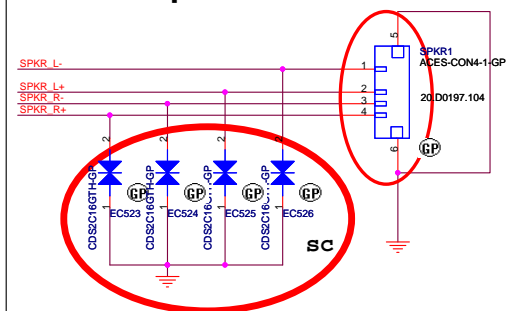
Internal Microphone



LINE OUT

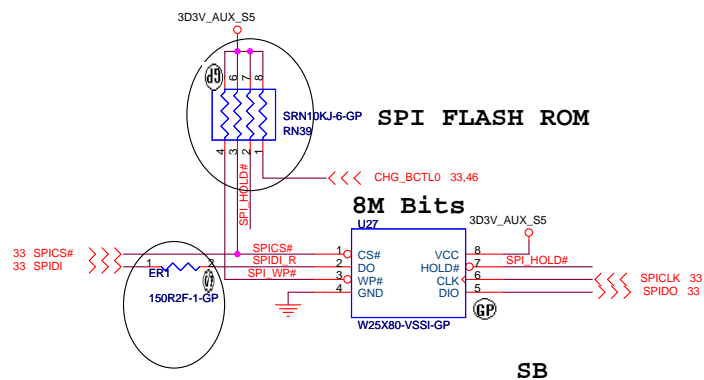


Internal Speaker



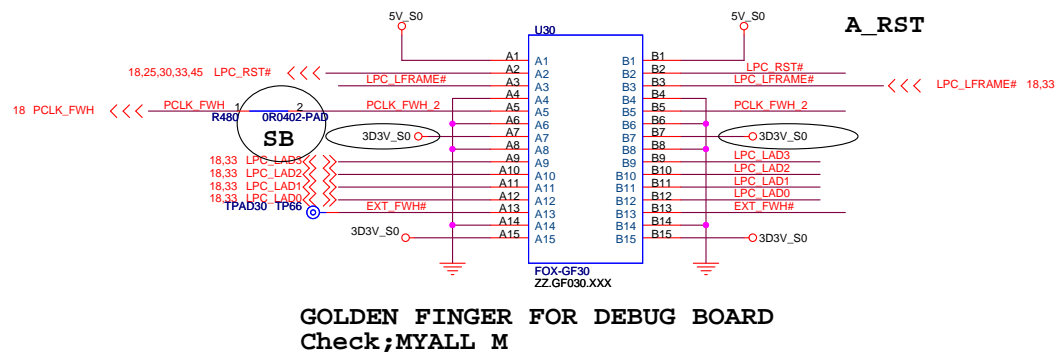
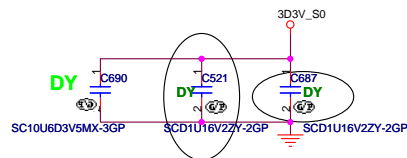
UMA			
緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
AUDIO AMP AND JACK			
Size	Document Number	Rev 1	
Date: Thursday, March 29, 2007		Sheet 32 of 49	
Pomona/Texteco			



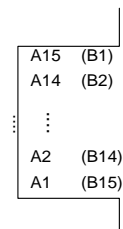


1. Add serial resistor 150 Ohm and Bypass Cap 4.7P on SPI_CLK(Close to KBC)
2. Add serial resistor 150 Ohm on SPI_DO(Close to KBC)
3. Add serial resistor 150 Ohm on SPI_DI(Close to SPI Flash)

Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46



TOP VIEW

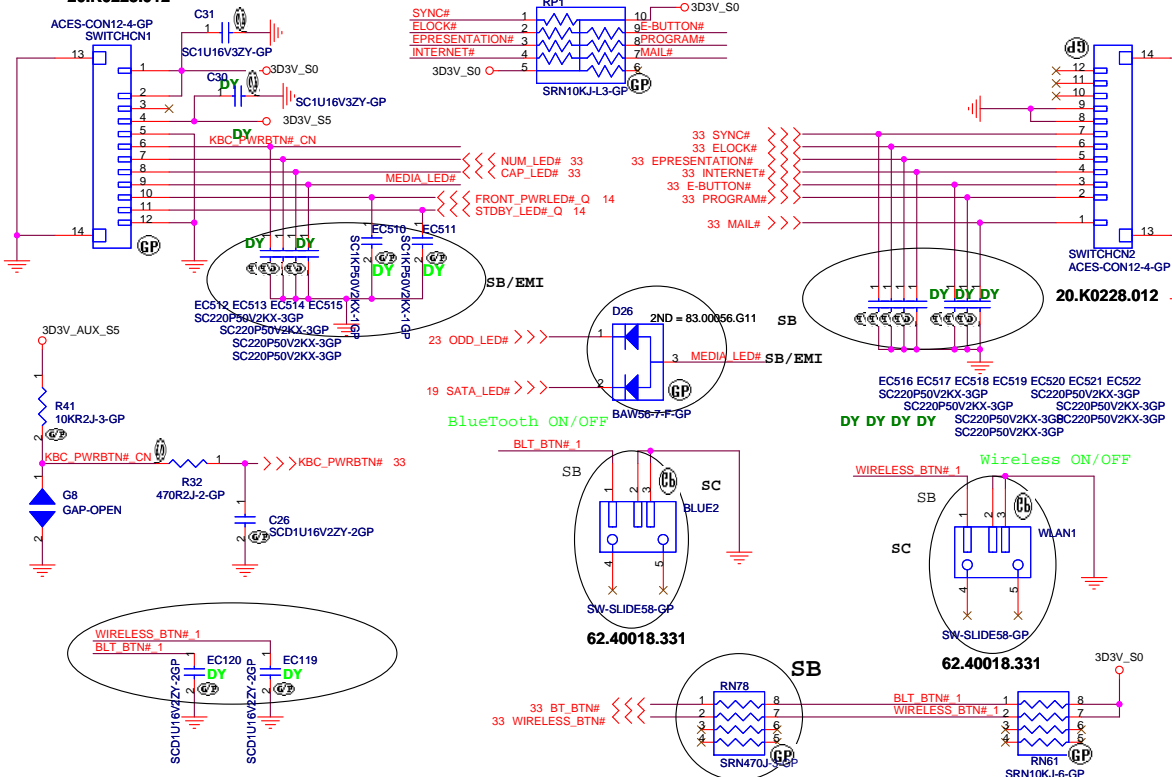


(BOTTOM VIEW)

UMA

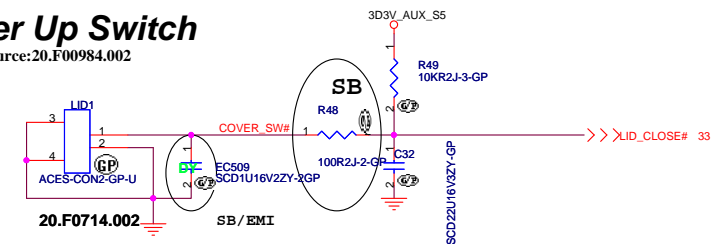
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
BIOS		
Size	Document Number	Rev
A3	Pomona/Textcoco	1
Date:	Thursday, March 29, 2007	Sheet 34 of 49

20.K0228.012

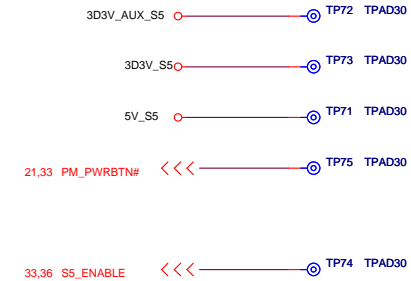


Cover Up Switch

2nd source:20.F00984.002

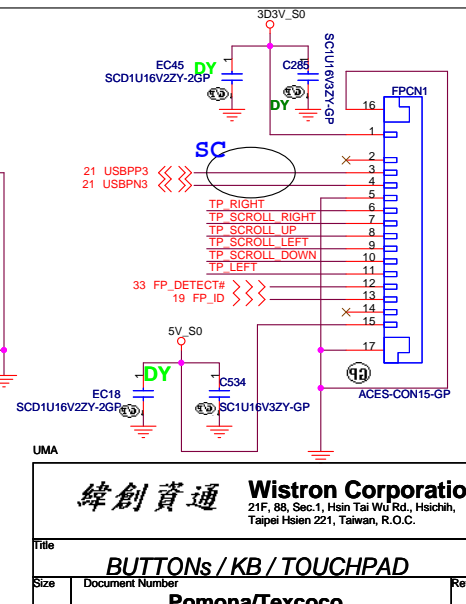
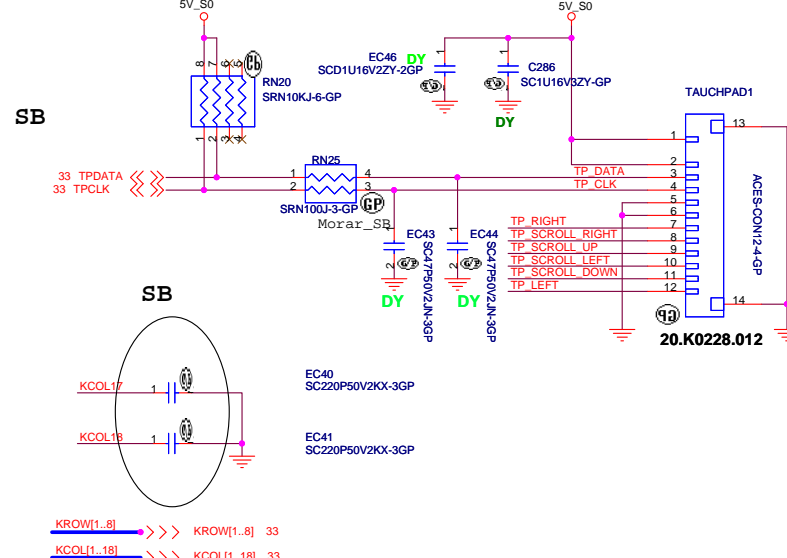
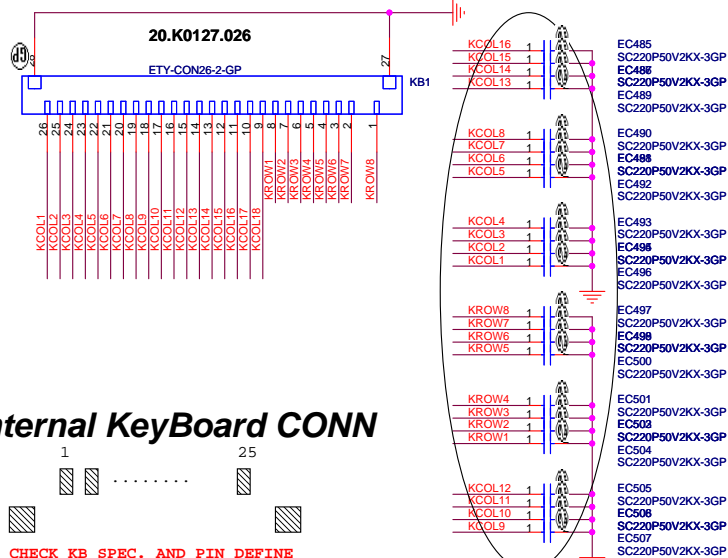


Check test point



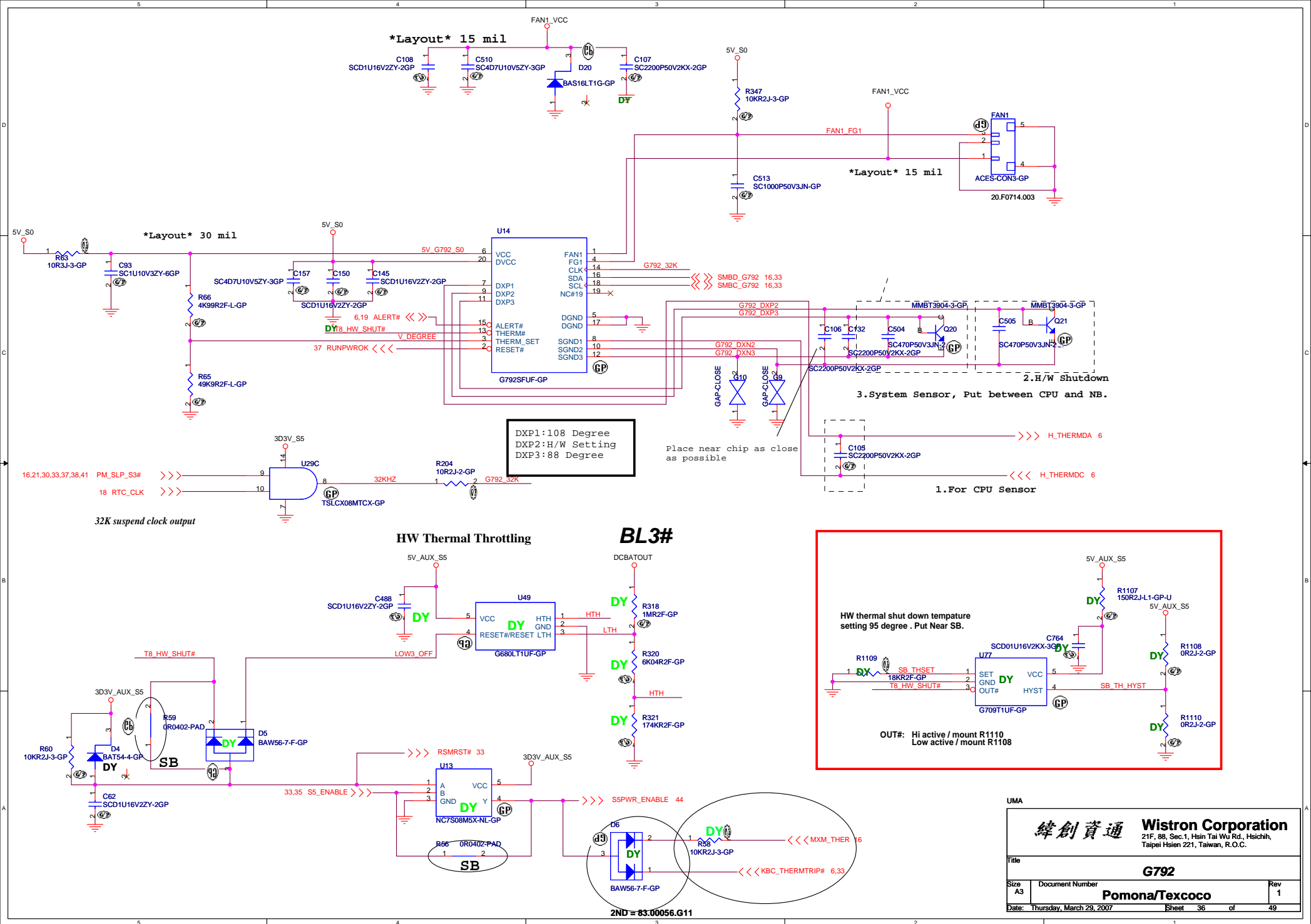
Test Point放在Dimm Door打開可量測處

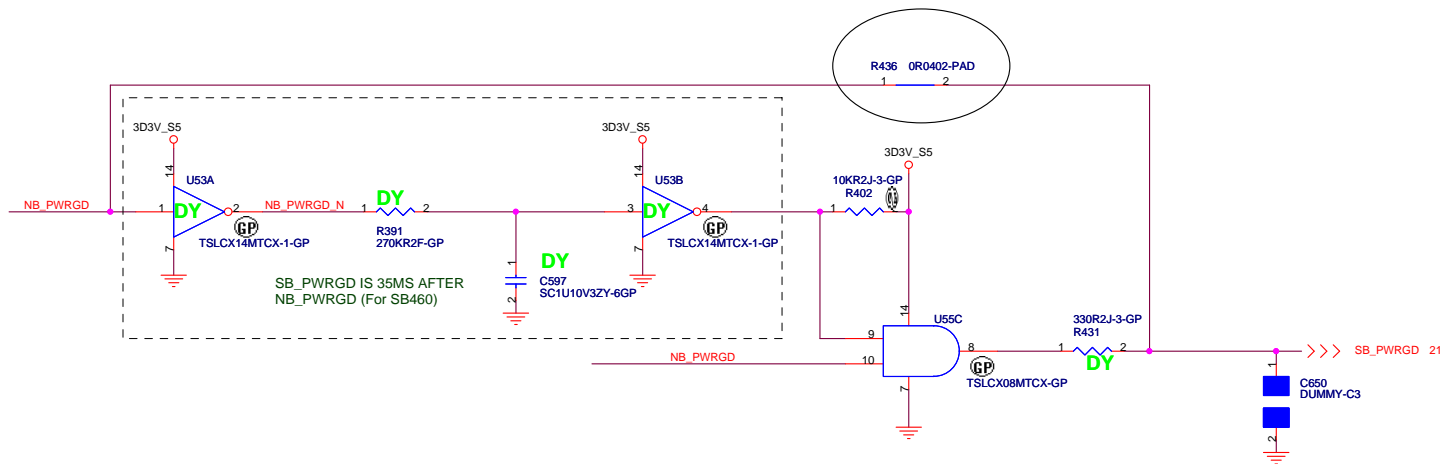
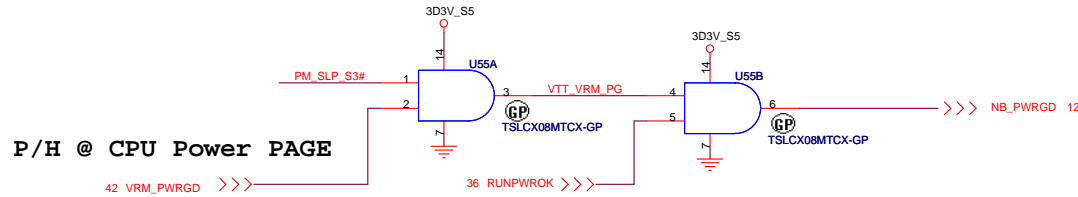
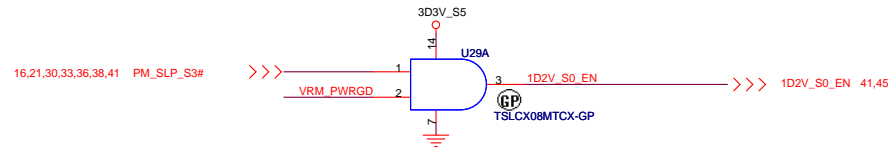
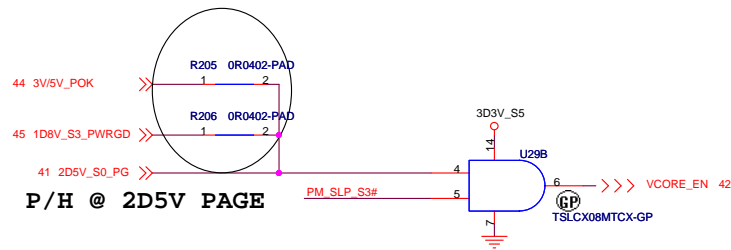
EMI Bypass cap.



緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **BUTTONs / KB / TOUCHPAD**
Size: Document Number: **Pomona/Textcoco** Rev: 1
Date: Thursday, March 29, 2007 Sheet 35 of 49

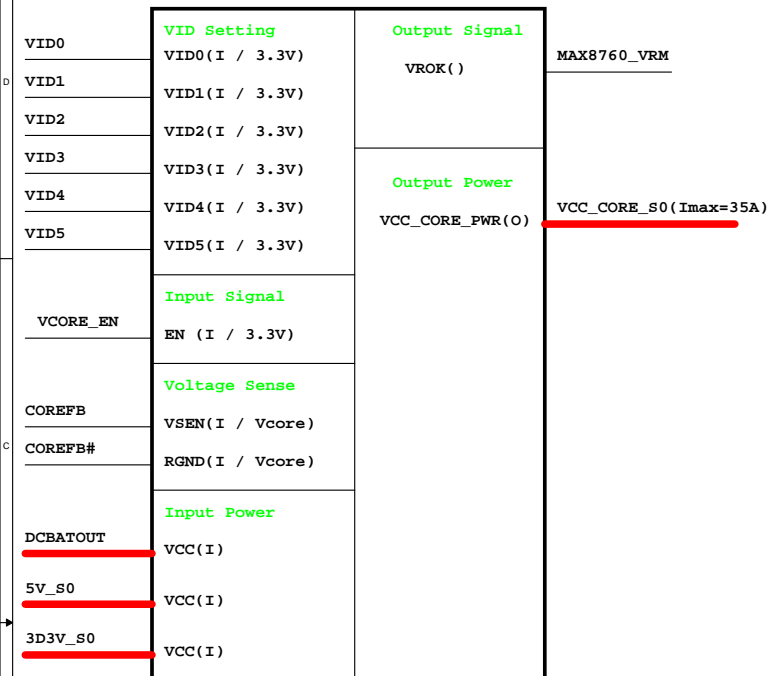




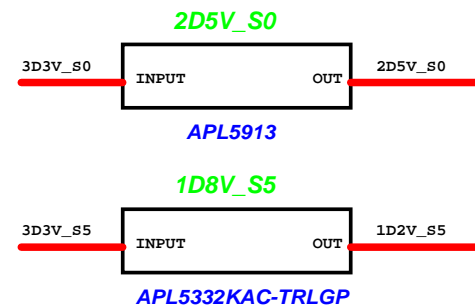
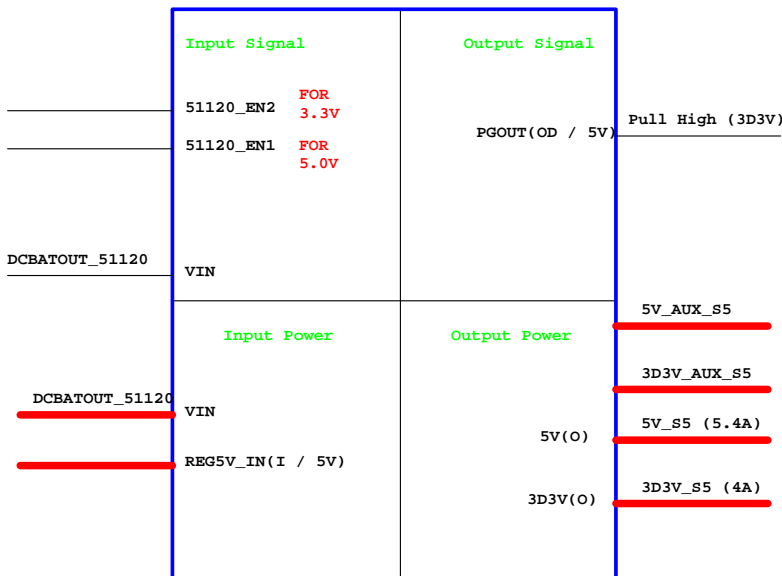


Date: Thursday, March 29, 2007 Sheet 38 of 49

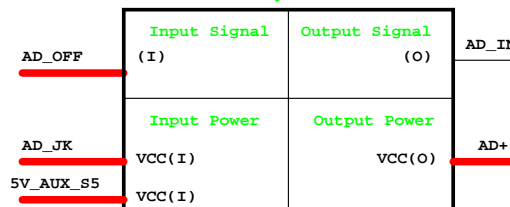
CPU_CORE
ISL6264CRZ



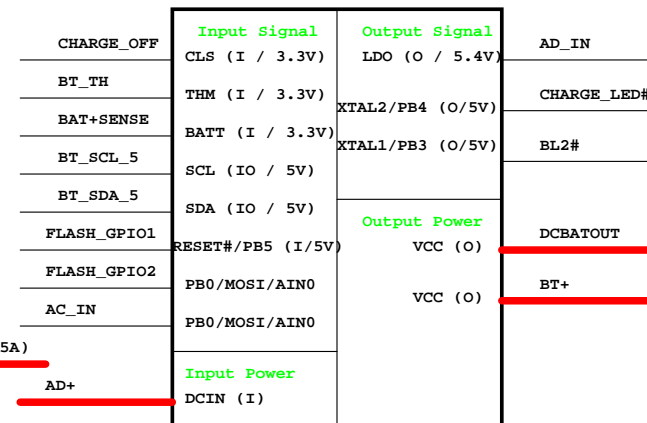
TI TPS51120
3D3V/5V



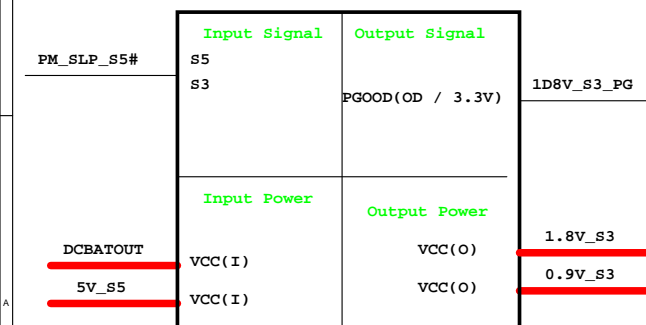
Adapter



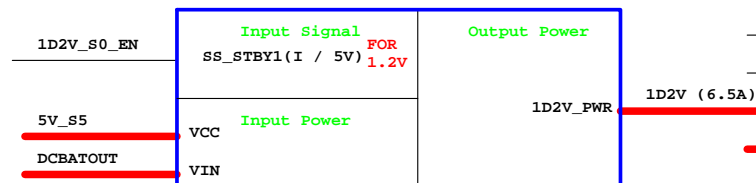
Charger_ISL6255



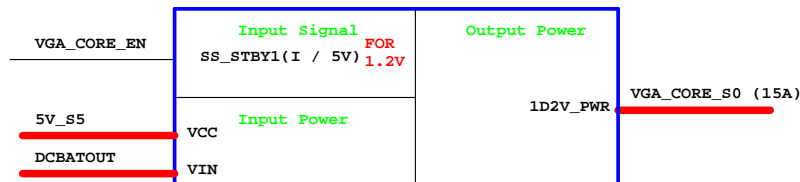
TI TPS51116
1.8V / 0.9V



ISL6268_1D2V



ISL6268_VGA_CORE

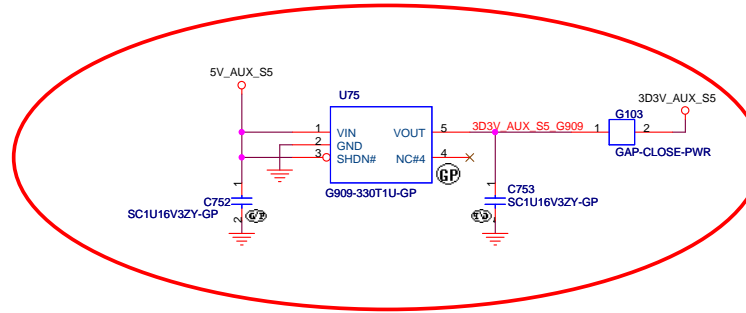


UMA

緯創資通 Wistron Corporation		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
Power Block Diagram		
Size A3	Document Number	Rev 1
Pomona/Texcoco		
Date: Thursday, March 29, 2007		

Aux Power 3D3V_AUX_S5

Aux Power 3D3V_AUX_S5

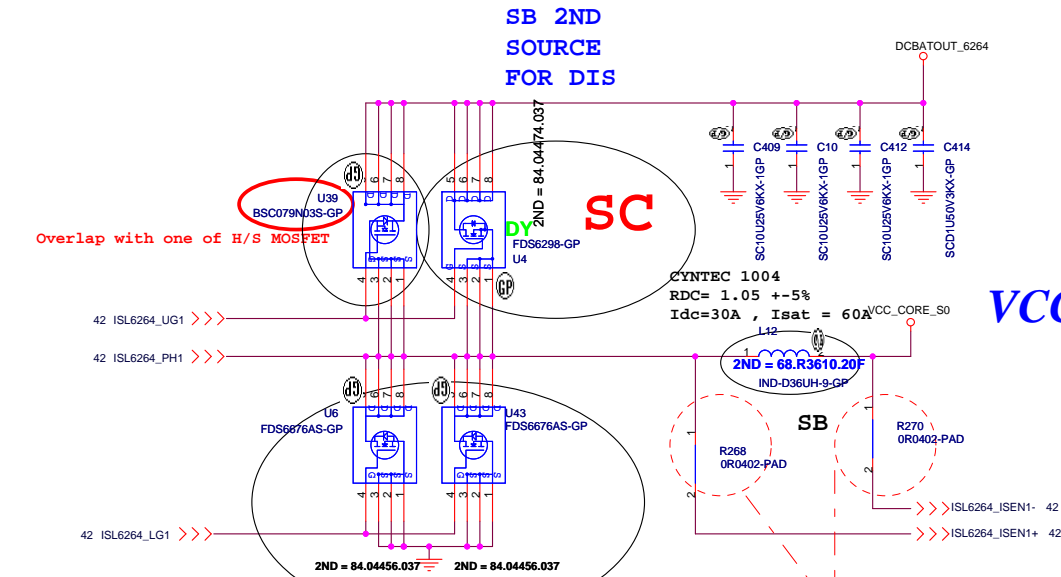


SB modify

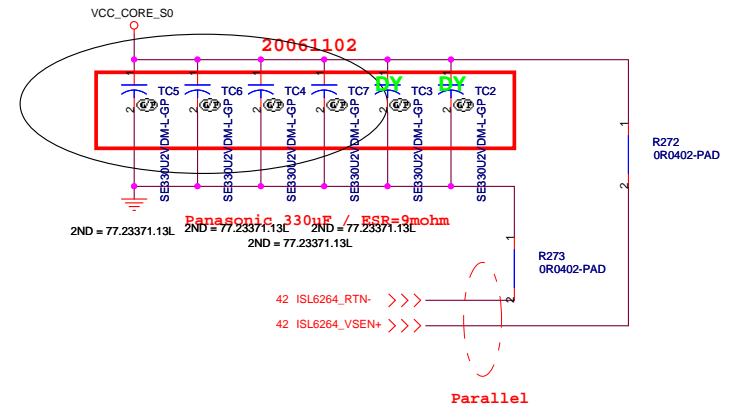
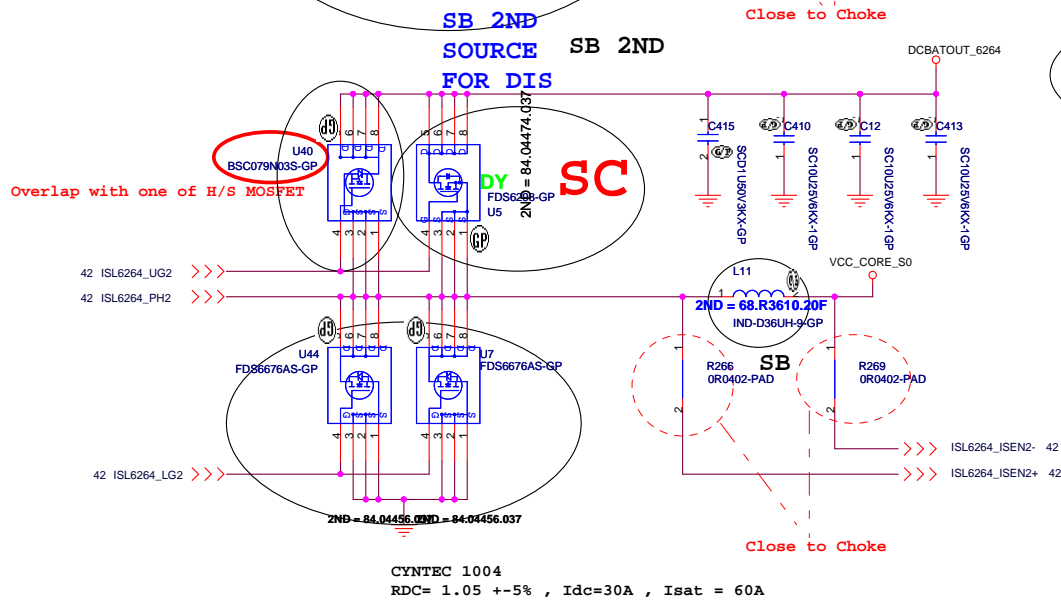
UMA			
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
3D3V AUX			
Size	Document Number		Rev
A3	Pomona/Textcoco		1
Date:	Thursday, March 29, 2007	Sheet 40 of 49	1

VID5	VID4	VID3	VID2	VID1	VID0	DAC
0	0	0	0	0	0	1.950
0	0	0	0	0	1	1.925
0	0	0	0	1	0	1.500
0	0	0	0	1	1	1.475
0	0	0	1	0	0	1.450
0	0	0	1	0	1	1.425
0	0	0	1	1	0	1.400
0	0	0	1	1	1	1.375
0	0	1	0	0	0	1.350
0	0	1	0	0	1	1.325
0	0	1	0	1	0	1.300
0	0	1	0	1	1	1.275
0	0	1	1	0	0	1.250
0	0	1	1	0	1	1.225
0	0	1	1	1	0	1.200
0	0	1	1	1	1	1.175
0	1	0	0	0	0	1.150
0	1	0	0	0	1	1.125
0	1	0	0	1	0	1.100
0	1	0	0	1	1	1.075
0	1	0	1	0	0	1.050
0	1	0	1	0	1	1.025
0	1	0	1	1	0	1.000
0	1	0	1	1	1	0.975
0	1	1	0	0	0	0.950
0	1	1	0	0	1	0.925
0	1	1	0	1	0	0.900
0	1	1	1	0	0	0.875
0	1	1	1	0	1	0.850
0	1	1	1	1	0	0.825
0	1	1	1	1	1	0.800
0	1	1	1	1	1	0.775
0	1	0	0	0	0	0.750
1	0	0	0	0	0	0.725
1	0	0	0	0	1	0.7125
1	0	0	0	1	0	0.7
1	1	1	1	1	1	0.375

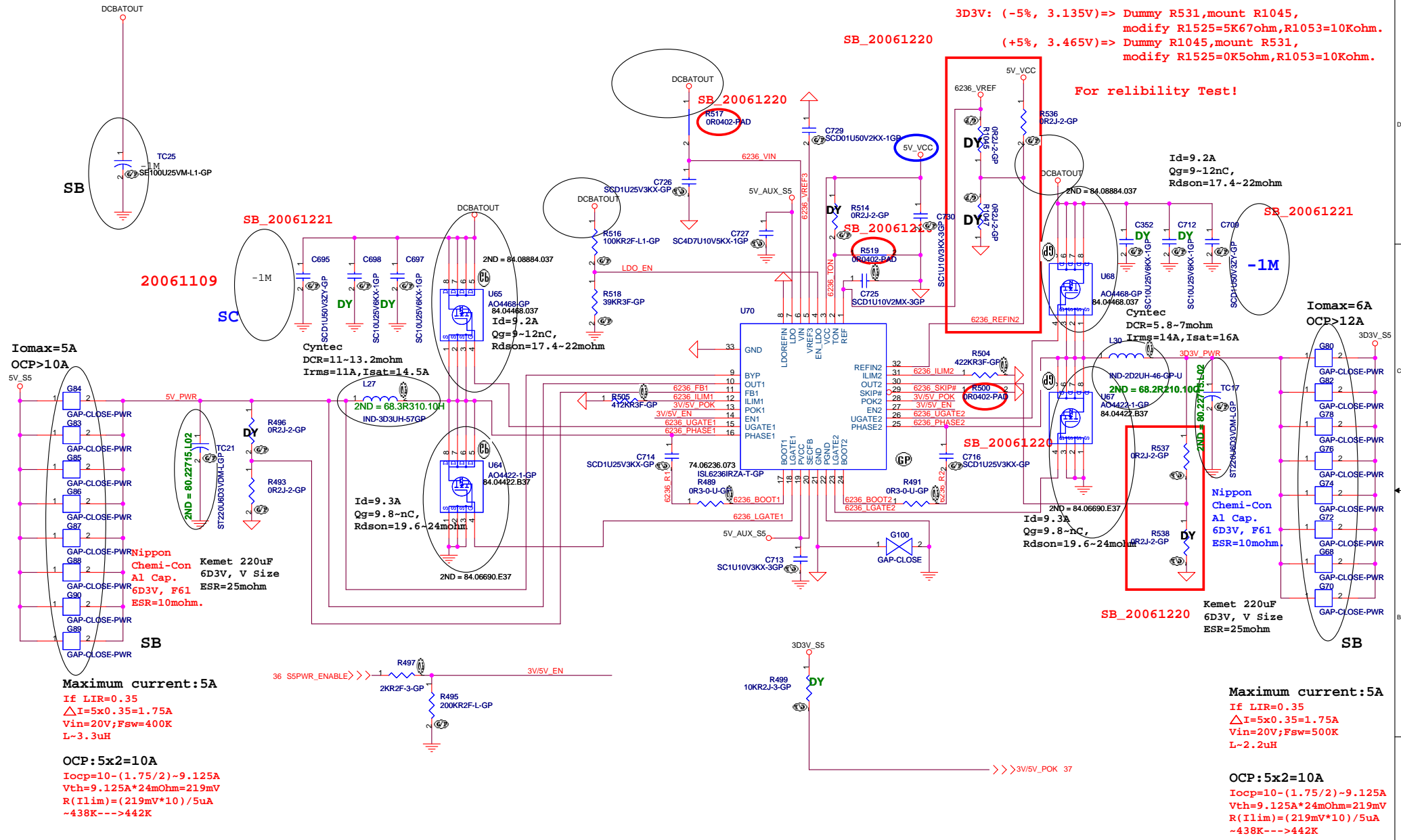




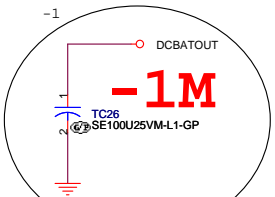
VCC_CORE_S0



UMA



UMA			
緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
ISL6236 5V 3D3V			
Size A3	Document Number		Rev 1
Pomona/Textcoco			
Date:	Thursday, April 19, 2007	Sheet 44 of	49



-1M

Id=9.6A
Qg=18-nC,
Rdson=13.5~16.5mohm

SB_20061221

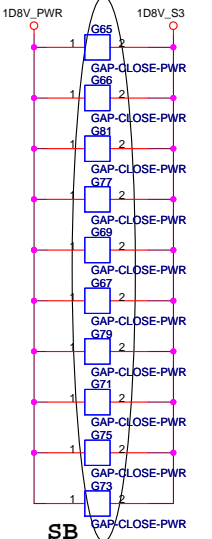
-1M

1D8V Iomax=8A
OCP>16A

Voutsetting=1.8046V

SC remove TC19

Nippon
Chemi-Con
Al Cap.
390uF/2D5V
ESR=15mohm



Id=13.2A
Qg=27nC,
Rdson=6.8~8.2mohm

PH at 2D5V Power Page

>>>1D8V_S3_PWRGD 37

PH at CPU Power Page

SB_20061220

Vout=0.758V*(R1+R2)/R2

SC

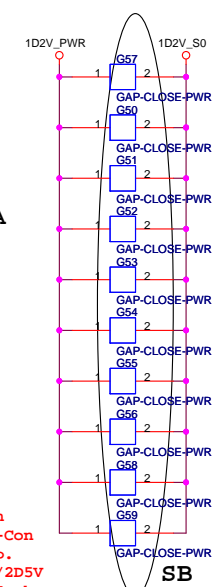
-1M

SB_20061221

-1M

1D2V Iomax=8A
OCP>16A

Voutsetting=1.2047V



Id=9.6A
Qg=18-nC,
Rdson=13.5~16.5mohm

SB CHANGE TO MOUNT ON UMA ONLY

12 STRP_DATA

STRP_DATA	1D2V(VCC_NB)
0	1.0
1	1.2

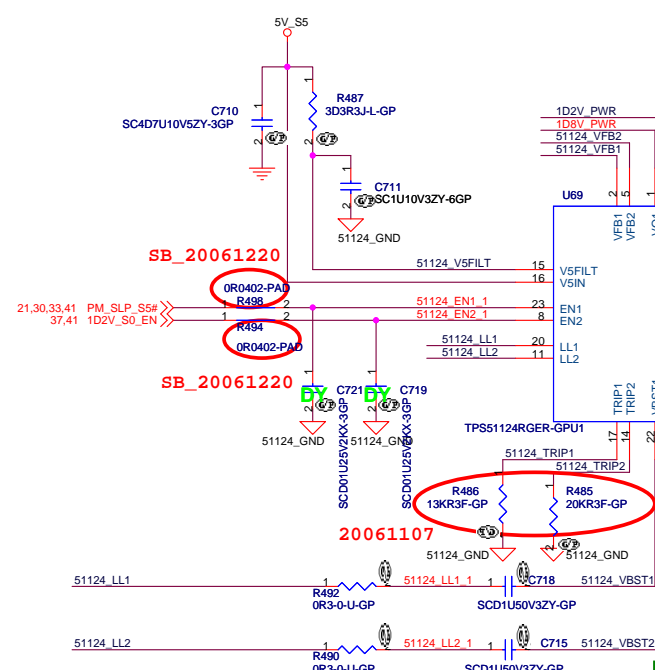
UMA

緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **TPS51124 1D8V 1D2V**

Size A3 Document Number **Pomona/Textcoco** Rev **1**

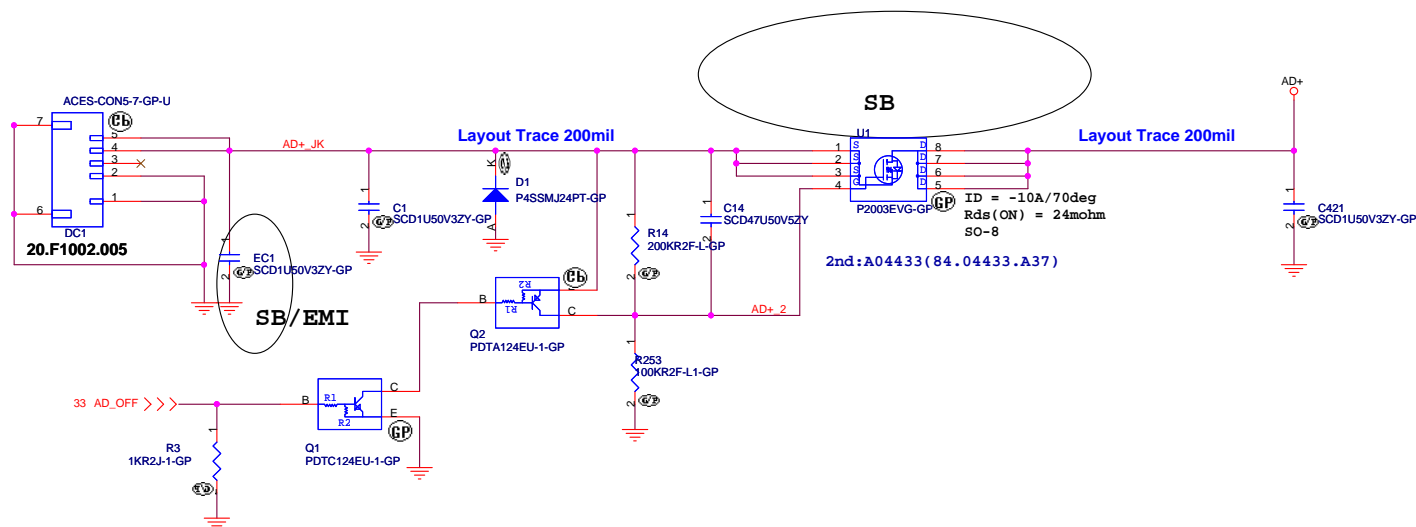
Date: Thursday, March 29, 2007 Sheet 45 of 49



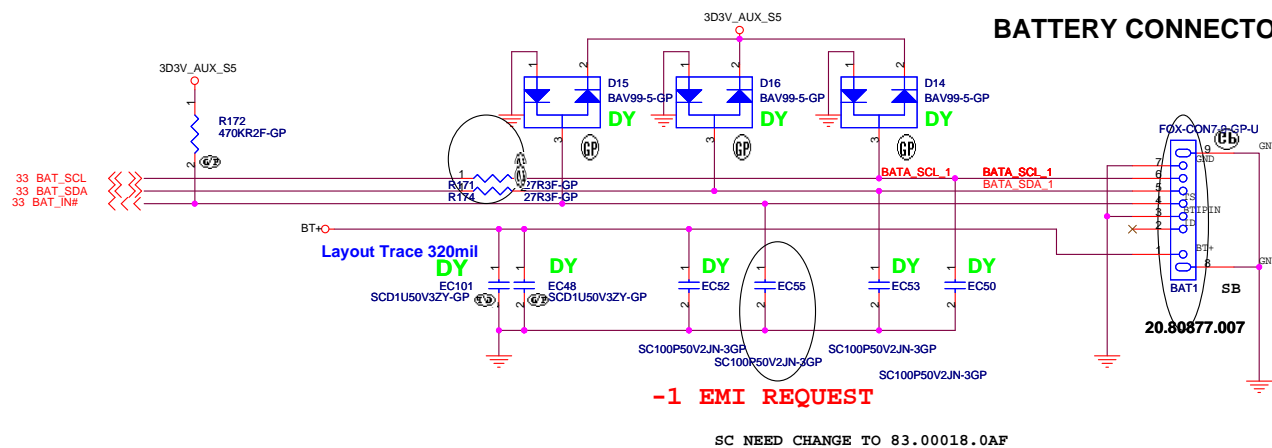
Vtrip(mV)=Rtrip(Kohm)*10(uA)
Iocp=(Vtrip/Rdson)+((1/(2*L*f))*(Vin-Vout)*Vout/Vin)

	GND	OPEN	V5FILT
TONSEL	230k/CH1 283k/CH2	283k/CH1 346k/CH2	346k/CH1 423k/CH2

Adaptor in to generate DCBATOUT



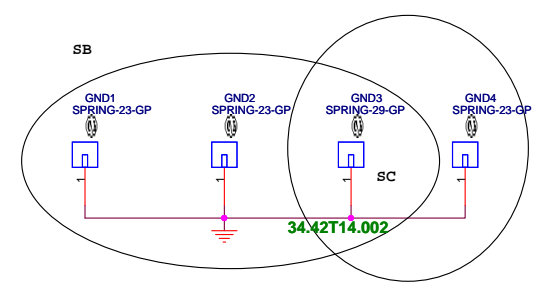
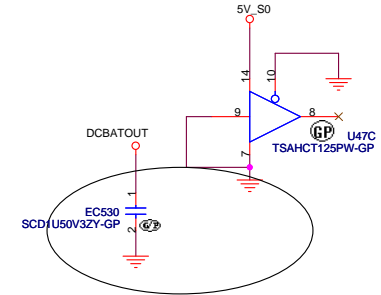
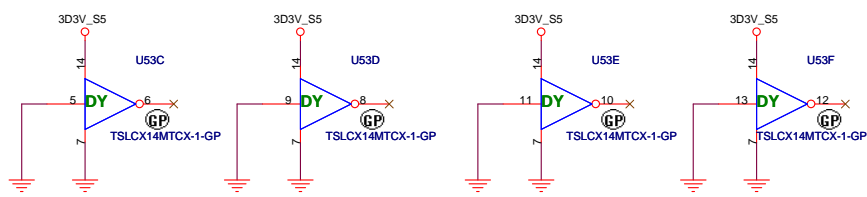
BATTERY CONNECTOR



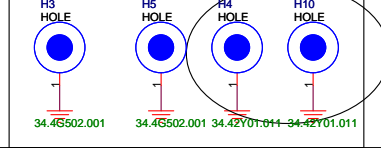
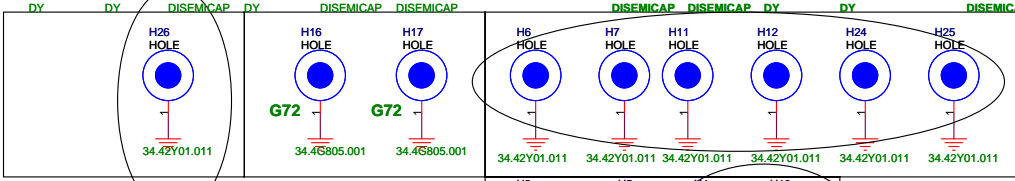
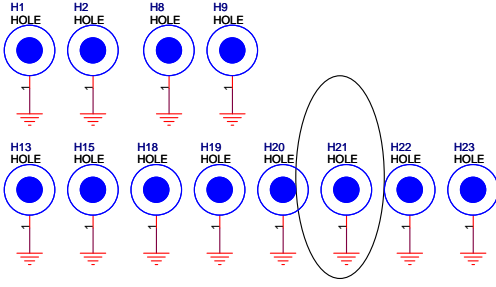
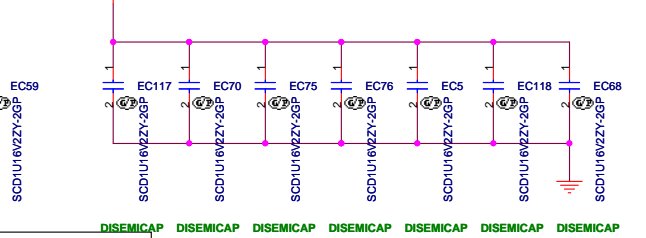
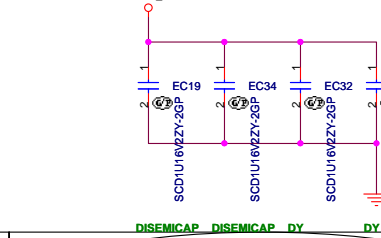
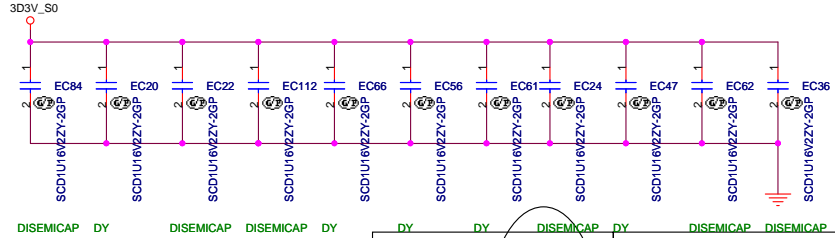
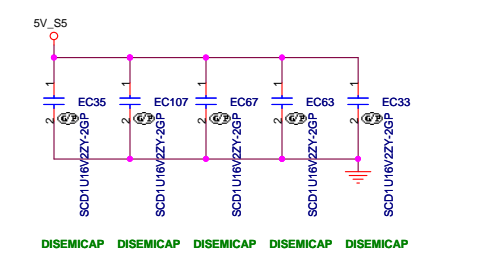
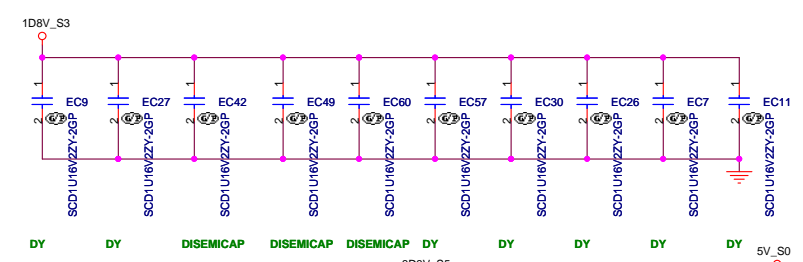
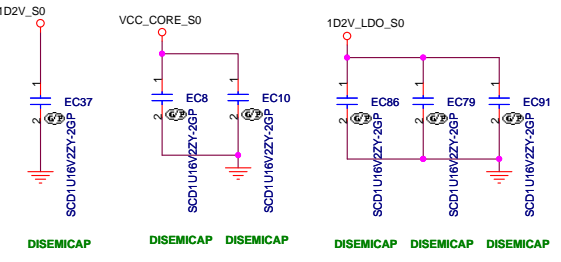
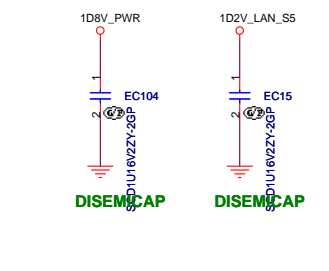
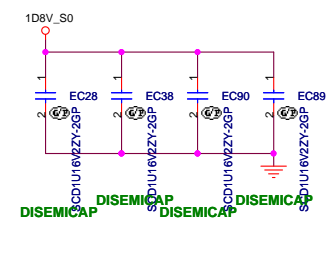
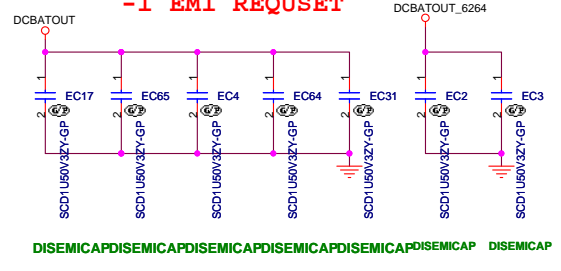
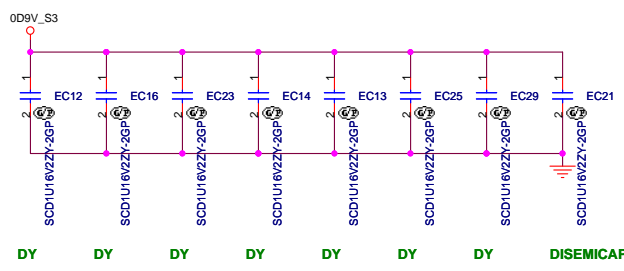
SC

UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title AD/BATT CONN	
Size A3	Document Number Pomona/Textcoco
Date: Thursday, March 29, 2007	Sheet 47 of 49
Rev 1	



-1 EMI REQUSET



孔徑要變更

UMA	
緯創資通 Wistron Corporation	
21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
EMI/Spring/Boss	
Size	Document Number
Pomona/Textcoco	
Date: Thursday, March 29, 2007	Sheet 48 of 49

PAGE3 DY RN21-24,RN34-RN36,R132,9LPR462AGLF INTERNAL P/D.
PAGE3 CHANGE X2,C307,C311 BY KDS SUGGESTION
PAGE14 ADD F2 BETWEEN DCBATOUT AND LCD CONN.
PAGE14 CHANGE LED2 TO DUAL COLOR LED FOR POWER LED AND STANDBY LED
PAGE14 CHANGE LED4 TO DUAL COLOR LED FOR CHARGER LED AND DC BATFULL LED
PAGE15 CHANGE C477,480,487 TO 15P FROM DY FOR SOLVE SIV ISSUE,DIS ONLY
PAGE15 CHANGE C477,480,487 TO 15P FROM DY FOR SOLVE SIV ISSUE,DIS ONLY
PAGE15 CHANGE C479,483,490 TO 15P FROM 6.8P FOR SOLVE SIV ISSUE.DIS ONLY;UMA WILL KEEP 6.8P
PAGE18 CHANGE X1,C259,C270 BY KDS SUGGESTION
PAGE19 CHANGE X5,C659,C656 BY KDS SUGGESTION
PAGE19 PSW_CLK# P/U 10K TO 3D3V_S5
PAGE21 CHANGE R101 TO DY FOR EC5WI#_KBC AND CHANGE TO R531 THAT CONNECT TO USB_OC6#(GEVENT6#)
PAGE23 CHANGE SATA1 CONN.
PAGE23 CHANGE ODD1 CONN.
PAGE24 CHANGE R27 TO 10R FOR SOLVE ACZ_SDATAIN1 OF SIV FAIL ITEM
PAGE25 CHANGE X4,C471,C472 BY KDS SUGGESTION
PAGE26 CHANGE RJ1 CONN.AND LAN_ACT_LED# TO B2 FROM A1,10M/100M/1G_LED# FROM B2 TO A3
PAGE26 CHANGE LAN_ACT_LED# TO B2 FROM A1
PAGE26 CHANGE 10M/100M/1G_LED# FROM B2 TO A3
PAGE28 CHANGE C691,C689 TO 6.8P BY KDS SUGGESTION
PAGE30 CHANGE NEW1 CONN.
PAGE30 CHANGE MINIC1 CONN.
PAGE30 ADD R537 AND SET TO DY
PAGE31 CHANGE R215 TO 27R FOR SOLVE ACZ_SDATAIN0 OF SIV FAIL ITEM
PAGE31 ADD R538 OR AND SET INTERNAL MIC TO LEFT CHANNEL,DY R224,D17 AND ADD D36
PAGE31 SET C391 TO DY FOR POP SOUND
PAGE31 CHANGE R247 TO 10K;R236 TO 6.8K;R248 TO DY;249 TO STUFF FOR SET GAIN TO 1.2W
PAGE31 CHANGE R238,239,242,243 TO 0R
PAGE31 CHANGE R223 TO STUFF
PAGE31 CHANGE INTMIC1 CONN.
PAGE31 CHANGE SPKR1 CONN.
PAGE33 ADD D35 BETWEEN KBC AND PM_PWRBTN#
PAGE33 DY R197 AND STUFF R193 FOR SET PCB VER. TO 001
PAGE33 CHANGE X3,C337,C341 BY KDS SUGGESTION
PAGE34 Add serial resistor 150 Ohm and Bypass Cap 4.7P on SPI_CLK(Close to KBC)
Add serial resistor 150 Ohm on SPI_DO(Close to KBC)
Add serial resistor 150 Ohm on SPI_DI(Close to SPI Flash)
PAGE33 CHANGE WLAN1,BLUE2 CONN.
PAGE37 SET R453 TO DY
PAGE38 ADD C750

-1

- 1.Change U19 ATIGLCK3 to SRCCLK3.PAGE3
- 2.Change U19 ATIGLCK2 to SRCCLK1.PAGE3
- 3.Add CLK14_SIO of U19;PIN62 FOR Super I/O.PAGE3
- 4.Change THERMTRIP# TO KBC GPI94.PAGE6
- 5.Change LDT_RST#;LDT_STP#;SB_CPUFWRGD P/L resistor to 680 ohms by AMD recommand.PAGE6
- 6.Adjust current limit resistor for FRONT_PWRLED.R1113 change to 68 ohms.PAGE14
- 7.Adjust current limit resistor for BT_LED.R251 change to 390 ohms.PAGE14
- 8.Adjust current limit resistor for DC_BATFULL_LED.R1116 change to 68 ohms.PAGE14
- 9.Add R1093 P/H 10K ohms TO 3D3V_S0 for slove WLAN_LED light leak in dos mode.PAGE14
- 10.Remove damping resistor of TMDS signal.PAGE16
- 11.Remove bridge resistor of TMDS signal.PAGE17
- 12.Change FP_DETECT TO KBC GPIO27.PAGE19
- 13.Change USB7 from PORT7 to PORT1 of U19.PAGE21
- 14.Change PCB_VER0/1 form KBC to GPIO4/5 of U19.PAGE21
- 15.Add ESD diode D38-D45 for USB signal.PAGE23
- 16.Add damping resistor 22 ohms and P/L CAP 22P for SD_CLK for EMI.PAGE27
- 17.Add P/L CAP 33P for SD/MMC_D0-D3 for EMI.PAGE29
- 18.Dummy R1062,R1058 and mount R1061 for MINICARD.PAGE30
- 19.Remove MIC array design.PAGE31
- 20.Add ESD diode EC523-526 for internal speaker.PAGE32
- 21.Add AD_DIFF on GPIO10 for separate 65W/90W adapter.PAGE33
- 22.Change KBC_MATRIX0# P/H to 3D3V_AUX_S5.PAGE33
- 23.Add SUPER IO circuit U76 for FIR function.PAGE33
- 24.BLON_OUT and BRIGHTNESS P/L cap close to KBC.PAGE33
- 25.Add R1089 to set BLON timing.PAGE33
- 26.Add U77 T8 shutdown circuit FOR U19(SB600).PAGE36
- 28.Change KBC_THERMTRIP# to KBC GPI94.PAGE36
- 29.Change value of R25.R26 and mount R17 to modify SUSTAND LOAD LINE to meet AMD spec.PAGE42
- 30.Add AD_DIFF for separate 65W/90W adapter.PAGE46
- 31.Add D46 and modify resistor value of R1111,R1112,R121,C294,C308 by vendor recommand.PAGE46

UMA			
Title			
<Title>			
Size	Document Number		Rev
A3	<Doc>		1
Date:	Thursday, March 29, 2007	Sheet	49 of 49